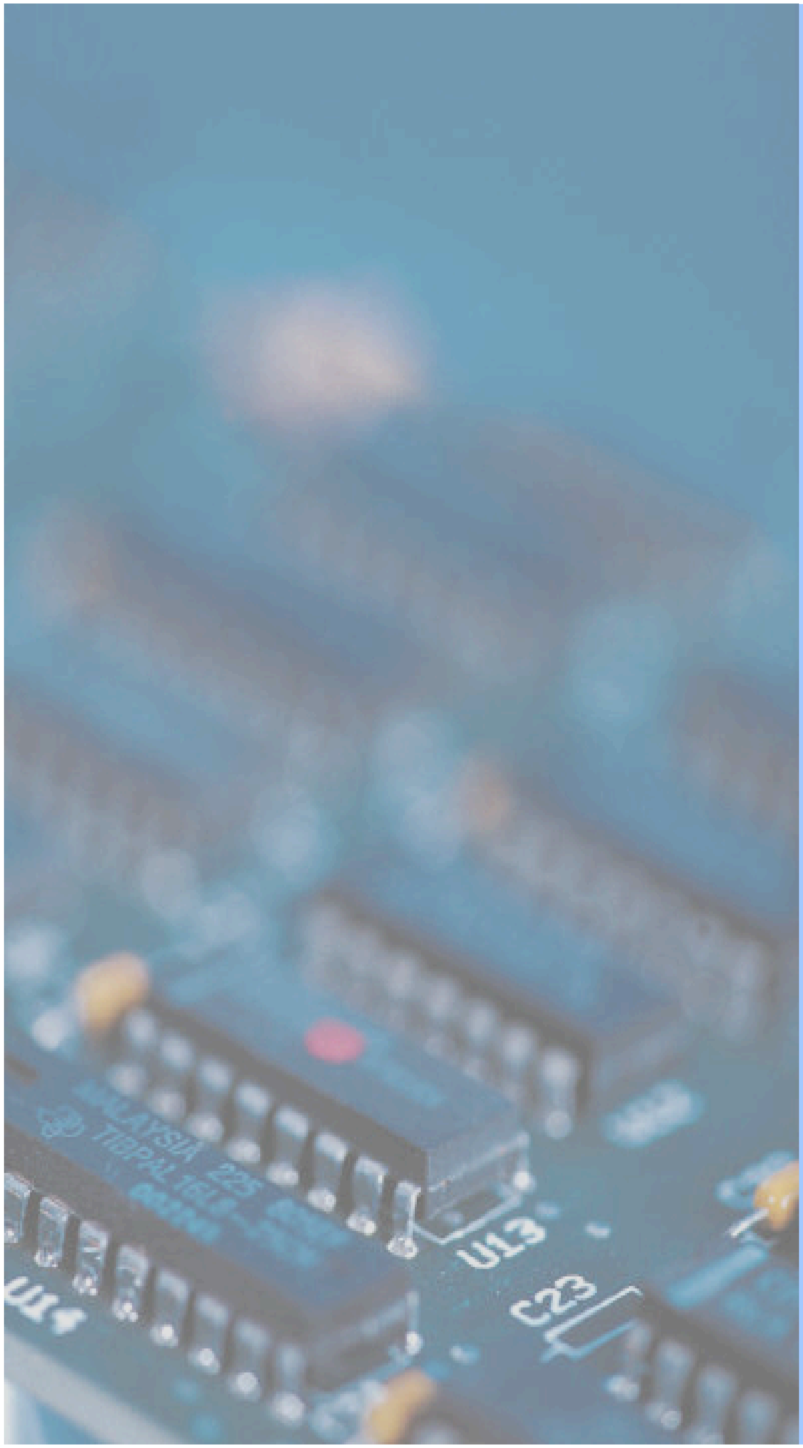


Prototyping Architectural Support for Program Rollback Using FPGAs

Radu Teodorescu

Josep Torrellas

http://iacoma.cs.uiuc.edu

University of Illinois

Summary

- Problem
  - Production software is hard to debug
- Solution
  - Always-on, lightweight debugger
  - Collect info about bug circumstances
  - Hardware support
- FPGA platform
  - Rapid prototyping
  - Design validation

Debugging Production Code

- Processor runs in two possible modes:
  - Normal
  - Speculative
    - Rollback capability
- Transition controlled by software
  - Special instructions

Debugging Production Code

```
num=a+b;
...
begin_spec();
p1=m[a[*x]]+a[m[&y]];
p2=&p1;
foo(p2);
...
if (rlbk_state) {
 collect[0]=&p1;
 collect[1]=&y;
}

end_spec(flag);
num=num+c;
...
```

non-speculative code

begin speculation

error-prone code

collect info on re-execution

end speculation

non-speculative code

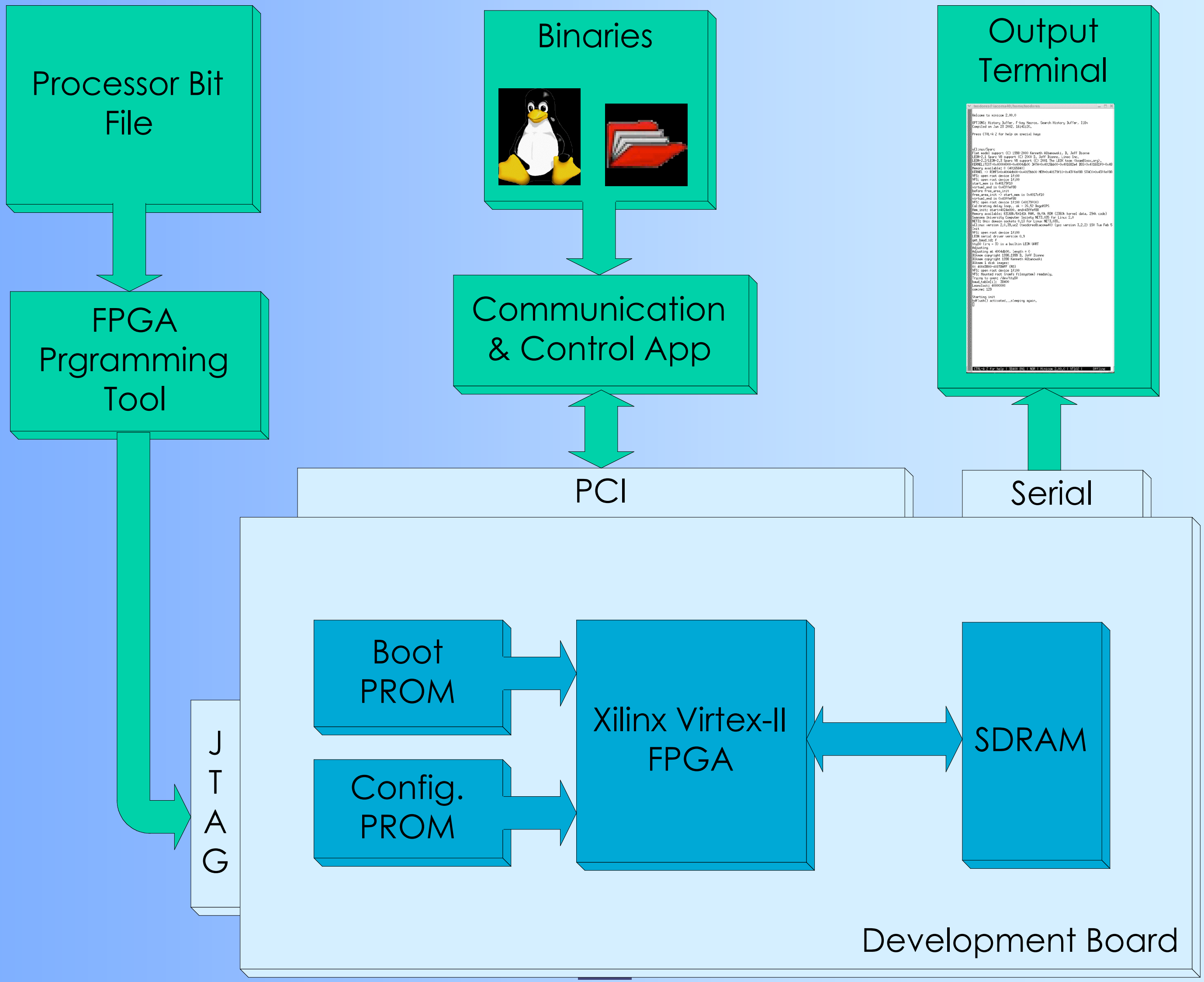
Hardware Support

New hardware	**Purpose**
Speculative cache	Buffer speculative data
Register checkpointing	Restore processor state
ISA support	Instructions to mark the speculative section
Performance counters	Feedback

Experimental Infrastructure

Baseline processor	SPARC V8 compliant In-order, single-issue, 5 stage pipeline Open source VHDL, Gaisler Research
Caches	1-4 set associative, 1-64KB/set
System on a Chip	PCI, Ethernet, serial interfaces
Development board	Xilinx Virtex II XC2V3000, 64 Mbytes SDRAM
Operating System	Linux embedded

FPGA System Architecture



```
Welcome to minicom 2.00.0

OPTIONS: History Buffer, F-key Macros, Search History Buffer, I18n
Compiled on Jun 23 2002, 16:41:20.

Press CTRL-A Z for help on special keys



uClinux/Sparc
Flat model support (C) 1998-2000 Kenneth Albanowski, D. Jeff Dionne
LEON-2.1 Sparc V8 support (C) 2000 D. Jeff Dionne, Lineo Inc.
LEON-2.2/LEON-2.3 Sparc V8 support (C) 2001 The LEOX team <team@leox.org>.
KERNEL:TEXT=0x40004000-0x4004db00 DATA=0x4015bb00-0x401682e4 BSS=0x401682f0-0x48
Memory available: 0 (40165840)
KERNEL -> ROMFS=0x4004db00-0x4015bb00 MEM=0x40179f10-0x43ffef88 STACK=0x43ffef88
VFS: open root device 1f:00
VFS: open root device 1f:00
start_mem is 0x40179f10
virtual_end is 0x43ffef88
before free_area_init
free_area_init -> start_mem is 0x4017cf10
virtual_end is 0x43ffef88
VFS: open root device 1f:00 (40179f00)
Calibrating delay loop.. ok - 26.52 BogoMIPS
Mem_init: start=4024e000, end=43ffef88
Memory available: 63168k/64141k RAM, 0k/0k ROM (2360k kernel data, 294k code)
Swansea University Computer Society NET3.035 for Linux 2.0
NET3: Unix domain sockets 0.13 for Linux NET3.035.
uClinux version 2.0.39.uc2 (teodores@iacoma40) (gcc version 3.2.2) 150 Tue Feb 5
Init
VFS: open root device 1f:00
LEON serial driver version 0.9
get_baud_id: f
ttyS0 (irq = 3) is a builtin LEON UART
Adjusting
Adjusting at 4004db00, length = 0
Blkmem copyright 1998,1999 D. Jeff Dionne
Blkmem copyright 1998 Kenneth Albanowski
Blkmem 1 disk images:
0: 4004DB00-4015BAFF (RO)
VFS: open root device 1f:00
VFS: Mounted root (romfs filesystem) readonly.
Trying to open: /dev/ttyS0
baud_table[i]:  38400
Leonclock: 40000000
comine: 129

Starting init
bdflush() activated...sleeping again.

CTRL-A Z for help | 38400 8N1 | NOR | Minicom 2.00.0 | VT102 |      Offline
```

Ongoing Work

- Operating system support
  - Extend speculation coverage
  - Kernel debugging
- Compiler support
  - Analysis and instrumentation
- Extend monitoring counters
  - Collect information that can help debugging

Conclusions

- We implemented a hardware prototype for software-controlled speculation
- Use it to debug production software
- FPGA platform
  - Validate the design
  - Experiment with real applications, including the Linux kernel
  - Evaluate hardware overhead

Prototyping Architectural Support for Program Rollback Using FPGAs

Contact:

Radu Teodorescu and Josep Torrellas

http://iacoma.cs.uiuc.edu