High Performance Energy Efficient Near Threshold Circuits: Challenges and Opportunities

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Era of Tera-scale Computing

Teraflops of performance operating on Terabytes of data

Performance

TIPS

GIPS

MIPS

KIPS

Dataset Size

Kilobytes

Megabytes

Gigabytes

Terabytes

Models

3D & Video

Multimedia

Text

Terascale

Multi-core

Single-core

Health

Personal Media Creation and Management

Entertainment, learning and virtual travel

Financial Analytics

Model-based Apps

Recognition

Mining

Synthesis

Text Models

Entertainment, learning and virtual travel

Financial Analytics

Model-based Apps

Recognition

Mining

Synthesis

Text Models
Tera-scale Platform Vision

- Scalable On-die Interconnect Fabric
- Special Purpose Engines
- Integrated IO devices
- Off Die interconnect
- Integrated Memory Controllers
- High Bandwidth Memory
- IO
- Socket Inter-Connect
# Silicon Process Technology Innovation

<table>
<thead>
<tr>
<th>Node Size</th>
<th>Year</th>
</tr>
</thead>
<tbody>
<tr>
<td>65nm</td>
<td>2005</td>
</tr>
<tr>
<td>45nm</td>
<td>2007</td>
</tr>
<tr>
<td>32nm</td>
<td>2009</td>
</tr>
<tr>
<td>22nm</td>
<td>2011</td>
</tr>
<tr>
<td>14nm</td>
<td>2013*</td>
</tr>
<tr>
<td>10nm</td>
<td>2015*</td>
</tr>
<tr>
<td>7nm</td>
<td>2017*</td>
</tr>
<tr>
<td></td>
<td>2019+</td>
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</table>

## Manufacturing Development

- **Hi-K**
- **Tri-Gate**

*Projected

Process innovation leads to energy efficient performance and predictable 2-year technology cycles.
22nm Performance and Energy Scaling

Transistor Performance and Power vs. Leakage

Innovation Enabled Technology Pipeline

32 nm 2009
22 nm 2011
14 nm 2013
10 nm 7 nm 5 nm 2015+

Manufacturing Development Research

Future options subject to change
Silicon Integration Providing Greater End-User Value

- More transistors/area: enables substantial system-on-chip integration opportunities
Extreme Scale (Exa-Scale) Computing Research

2W - 100 GigaFLOPS

20MW - ExaFLOPS

10 year goal: ~300X Improvement in energy efficiency

Equal to 20 pJ/FLOP at the system level

J. Rattner, ISCA 2012 Keynote
Ultra Low Power Graphics/Video & Security Circuits

DSP functions highly throughput-oriented: Amenable for parallelism/pipelining
⇒ Better power-performance optimization
⇒ Optimal partitioning of tasks between GP processor and dedicated engines
Specialized HW Accelerators for Exa-Scale

General purpose cores, special-purpose accelerators, interconnect fabric

**Efficient, adaptive, reconfigurable, resilient**

Fixed function vs. limited programmability

Operation over wide supply voltage range (near-threshold to nominal)
NTV Operation & Energy Efficiency

Frequency reduces almost linearly first, then exponentially.
Total power reduces by three to four orders of magnitude.

Energy efficiency improves by one order of magnitude at NTV.
Energy efficiency reduces in subthreshold operation.
Leakage power reduces by two to three orders of magnitude.

H. Kaul, R. Krishnamurthy et al, ISSCC 2008
NTV Across Technology Generations

H. Kaul, et. al., ISSCC 2009

S. K. Hsu, et. al., ISSCC 2012

A. Agarwal, et. al., ISSCC 2010

NTV operation improves energy efficiency across 45nm-22nm CMOS
NTV Opportunities for Wide Dynamic Range

Penwell CPU Dynamic Range

- Core Freq = 1.3 GHz
  Power: ~500mW
- Core Freq = 600MHz
  Power: ~175mW
- Core Freq = 100MHz
  Power: ~50mW

Burst

Ultra-LFM

LFM

HFM

Fine-grained power management through dynamic voltage & frequency scaling

Power assumptions: Tj=70°C, Steady State Worst Case ST App Power
Projected on Intel 32nm process

T. Thakkar, Intel Developer Forum 2012
ATOM™ 32nm SOC V/F Islands

SoC integration of many unrelated functions in their own power ‘islands’.

- On-die voltage regulation leading to power ‘islands’ that can have different voltage levels.
- Power management that shuts functional units off.
- Voltage-Frequency pairs; CPU’s can be run in several operating points where its power supply is adjusted to reduce power while keeping various functional blocks at constant voltage:
  - lowest frequency: 100 - 600MHz
  - medium frequency: 700 - 1500MHz
  - burst frequency: 1600 – 2500MHz
- OFF chip drivers have to support various voltage levels whereas the controller logic is powered by a lower voltage:
  - LPDDR: 1.25V
  - MIPI-display: 1.25V
  - HDMI-display 3.3V
  - SD cards: 2.85V
  - GPIO: 1.25V, 1.80V
NTV Opportunities for Converged Core

Design Philosophy

Retain key prior Sandy Bridge and Ivy Bridge microarchitecture features, such as: Intel® Hyper-Threading, Intel® Turbo Boost, Ring Interconnect

Converged core: Single microarchitecture that scales from tablet to server

Performance
- Legacy Code Performance Improvements
- New Technologies to Extract Greater Parallelism

Modularity
- Increased power/performance range
- Greater number of supported products
- Support for SoC designs

Power Innovations
- Active Power Reduction
- Idle Power Reduction
- Focused on Full Platform, not just CPU

Goal: Achieve new levels of power reduction without compromising performance

T. Piazza, Intel Developer Forum 2012
Impact of Variation on NTV

$$frequency \propto \frac{(V_{dd} - V_t)^\alpha}{V_{dd}}$$

5% variation in Vt or Vdd results in up to 50% variation in circuit performance
Monte-Carlo Simulations
18% nominal frequency spread
2X spread at NTV

65nm CMOS measurements
5% nominal spread due to temperature
2X spread at NTV

H. Kaul, R. Krishnamurthy et al, ISSCC 2008
Using Vdd to Compensate for Variation

- Adaptive Voltage Compensation for variation tolerance
- Adjust supply voltage to maintain constant performance
- $\pm 50\text{mV}$ adjustment about 320mV:
  - Nominal 23MHz performance sustained across 0-110°C and fast-slow skews
Subthreshold Leakage at NTV

NTV operation reduces total power, improves energy efficiency.
Subthreshold leakage power is substantial portion of the total.
Low Voltage SRAM and Register File

6T SRAM suffers stability and yield at NTV

6T SRAM cell with larger transistors
8T/10T SRAM for improved stability and yield

Variation tolerant register file for NTV

Conventional dual-ended (DE) write cell
(Write failure due to strong P and weak N)

Dual-ended transmission gate (DETG) write cell

S. Hsu, R. Krishnamurthy et al, ISSCC 2012
Low Voltage Latches and Flip-flops

Designing flip-flops for NTV

Upsized

Non-minimum Channel Length

Averaging with vector flip-flops

Vmin improves by 175 mV
Hold time margin by 7 to 30%

Shared min-sized clock drivers
Low Voltage Logic: Multiplexers & Gates

Designing multiplexers for NTV

One-hot 4:1

Encoded 4:1

Transmission gates, logic gates
Issue:
Large off-current paths
Weak on-current paths
Body effect

Up to 3X reduction in worst case static droop

Avoid series connected transmission gates

Logic fan in limited to 3 stack
Low Voltage Level Converters

CVSL Level Converter
Significant energy consumed in contention currents

Two-stage cascaded split-output level shifter
CVSL split into two stages to reduce contention current
Decoupled output for smaller CVSL
20% energy reduction

Ultra-low voltage split-output level shifter
Decoupled output from CVSL
Interrupts contention devices
Vmin improved by 125 mV

H. Kaul, R. Krishnamurthy et al, ISSCC 2009
## Soft Errors and Reliability

### Voltage (V)

**n-SER/cell (sea-level)**

- 65nm
- 90nm
- 130nm
- 180nm
- 250nm

Soft error/bit reduces each generation

Impact of NTV on soft error rate

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### Technology (nm) Relative to 130nm

- Latch
- Memory

Assuming 2X bit/latch count increase per generation

Soft error at the system level will continue to increase

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### Positive impact of NTV on reliability

- Low V → lower E fields, low power → lower temperature
- Device aging effects mitigated
- Lower electro-migration related defects
NTV SIMD Permutation Engine

256b Permutation Engine Organization

- SIMD permutation operations are key for maximizing vector datapath utilization in multimedia, graphics, and signal processing workloads

- SIMD vector permutation engine with 2-dimensional shuffle consists of register file for vertical shuffle and permutation crossbar for horizontal shuffle

<table>
<thead>
<tr>
<th>Process</th>
<th>22nm CMOS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Nominal Vcc</td>
<td>0.9V</td>
</tr>
<tr>
<td>Permute Xbar</td>
<td>256b byte-wise any-to-any</td>
</tr>
<tr>
<td>Register File</td>
<td>32x256b 3R/1W</td>
</tr>
<tr>
<td>Die Area</td>
<td>0.048mm²</td>
</tr>
<tr>
<td>Pad Count</td>
<td>30</td>
</tr>
</tbody>
</table>
Logic and Memory $V_{\text{MIN}}$ Circuit Optimizations

- Register file and logic $V_{\text{MIN}}$ circuit optimizations enable NTV operation
- Register file $V_{\text{MIN}}$ techniques: (i) clock-less static CMOS reads, (ii) dual-ended transmission gate (DETG) writes with shared P/N
- Logic $V_{\text{MIN}}$ techniques: (i) vector flip-flops, (ii) stacked min-delay buffers, (iii) shared gates to average min-sized transistor variation, (iv) ultra low voltage split-output level shifters
22nm Simulations/Measurements

**Register File** $V_{\text{MIN}}$ Simulations

- 22nm $V_{\text{MIN}}$ simulations performed at 0°C - 85°C
- 3σ systematic, 6σ random variation

<table>
<thead>
<tr>
<th>$V_{\text{MIN}}$ (mV)</th>
<th>3σ</th>
<th>4σ</th>
<th>5σ</th>
<th>6σ</th>
</tr>
</thead>
<tbody>
<tr>
<td>Read</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Dynamic</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Static</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Write</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>DET cell</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>DETG cell</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>DET shared P/N cell</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

22nm $V_{\text{MIN}}$ improvements: register file $V_{\text{MIN}}$ by 250mV and logic $V_{\text{MIN}}$ by 150mV

- Nominal: 1.8GHz, 0.9V, 50°C down to sub-threshold: 16.8MHz, 280mV
- Wide voltage supply scalability across 280mV - 1.1V increasing energy efficiency by 9x: **Industry’s first Tri-Gate NTV Logic + Memory circuits**

S. Hsu, R. Krishnamurthy et al, ISSCC 2012 & JSSC January 2013
NTV Variable Precision FPU

Accelerator for Smarter Numerics: Variable Precision FP

- Today’s floating-point units wastes energy, time, and storage by using worst-case precision everywhere
- Alternative: use a variable-precision floating point prototype unit with accuracy tracking for multiply-add
- Changing precision (24-bit $\rightarrow$ 12-bit $\rightarrow$ 6-bit) on-the-fly can cut energy by 50%

H. Kaul, R. Krishnamurthy et al, ISSCC 2012
# Experimental NTV Processor

**Technology**
- 32nm High-K Metal Gate
- 1 Poly, 9 Metal (Cu)
- 6 Million (Core)
- 2mm²

**Packaging**
- 951 Pin FCBGA Package
- Custom Interposer

**Legacy Socket-7 Motherboard**

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NTV Design Methodology

Normalized Delay Slowdown Due to Random Variations (6σ)

Complex, High Stacked Logic Gates

Nominal Versus High Vt Devices

Wide Transmission Gate Multiplexers

Minimum/Small Sized Devices

Nominal Vt • High Vt

2 Stack □ 3 Stack • 4 Stack

2 Wide □ 3 Wide • 4 Wide

76% 108%

127% 130%

0.2 0.3 0.4 0.5 0.6 0.7 0.8 0.9 1 1.1

Logic Vcc (V)

Logic Vcc (V)

0.2 0.3 0.4 0.5 0.6 0.7 0.8 0.9 1 1.1

0.2 0.3 0.4 0.5 0.6 0.7 0.8 0.9 1 1.1

0.2 0.3 0.4 0.5 0.6 0.7 0.8 0.9 1 1.1

0.2 0.3 0.4 0.5 0.6 0.7 0.8 0.9 1 1.1

2X 3X 4X 5X

Device Width

0.5V
Power & Performance

32nm CMOS, 25°C

Subthreshold Power & Performance

Total Power (mW) vs. Frequency (MHz)

Logic Vcc / Memory Vcc (V)

Subthreshold: 1% Logic leakage, 4% Logic dynamic, 33% Memory leakage

NTV: 27% Logic leakage, 15% Logic dynamic, 53% Memory leakage

Super-threshold: 11% Logic leakage, 3% Logic dynamic, 81% Memory leakage
# Wide Dynamic Range

<table>
<thead>
<tr>
<th>ENERGY EFFICIENCY</th>
<th>VOLTAGE</th>
<th>Ultra-low Power</th>
<th>Energy Efficient</th>
<th>High Performance</th>
</tr>
</thead>
<tbody>
<tr>
<td>LOW</td>
<td>LOW</td>
<td>280 mV</td>
<td>0.45 V</td>
<td>1.2 V</td>
</tr>
<tr>
<td>ZERO</td>
<td>MAX</td>
<td>3 MHz</td>
<td>60 MHz</td>
<td>915 MHz</td>
</tr>
<tr>
<td>~5x Demonstrated</td>
<td>~5x</td>
<td>2 mW</td>
<td>10 mW</td>
<td>737 mW</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1500 Mips/W</td>
<td>5830 Mips/W</td>
<td>1240 Mips/W</td>
</tr>
</tbody>
</table>
Compute energy reduces faster than global interconnect energy
For constant throughput, NTV demands more parallelism
Increases data movement at the system level
System level optimization is required to determine NTV operating point
Improving Efficiency of the On-Die Network

M. Anders, R. Krishnamurthy et al, ISSCC 2010
Hybrid Circuit-/Packet-Switched Network

- Circuit-switching eliminates intra-route data storage
- Packet-switching used only for channel requests
- 2.5X to 3X better efficiency over packet switched network
Fine-grain Reconfigurable Fabrics

Reconfigurable Fabric Array (RFA)

Reconfigurable fabric tightly coupled to processor pipeline

Reconfigurable fabric directly interfaced with memory
- Optimized for arithmetic with support for random logic
  - Four 3-input Look-Up Tables (LUTs)
  - Three 4b adders
- 27 inputs, 15 outputs, 43 configuration bits
# 32nm High-K/Metal-Gate CMOS Die Micrograph

![Micrograph Image]

<table>
<thead>
<tr>
<th>Process</th>
<th>32nm High-K Metal-Gate CMOS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Nominal Supply</td>
<td>1.0V</td>
</tr>
<tr>
<td>Interconnect</td>
<td>9 metal Cu</td>
</tr>
<tr>
<td>Number of CLBs</td>
<td>6</td>
</tr>
<tr>
<td>Register File Array</td>
<td>64-entry x 32b</td>
</tr>
<tr>
<td>Die Area</td>
<td>0.076mm²</td>
</tr>
<tr>
<td>Number of Transistors</td>
<td>110K</td>
</tr>
<tr>
<td>Pad Count</td>
<td>30</td>
</tr>
</tbody>
</table>
255mV (Sub-threshold) operation in 32nm CMOS technology

*Industry’s first ultra-low-voltage reconfigurable accelerator*

A. Agarwal, R. Krishnamurthy et al, ISSCC 2010
1.5mm³ Intraocular Pressure Monitor

- Continuous IOP monitoring
- Wireless communication
- Energy-autonomy
- Device components
  - Solar cell
  - Wireless transceiver
  - Cap to digital converter
  - Processor and memory
  - Power delivery
  - Thin-film Li battery
  - MEMS capacitive sensor
- Biocompatible housing

Courtesy: Gregory Chen, U. Michigan
Summary

• Moore’s Law has fueled the worldwide technology revolution for over 40 years and will continue for at least another decade
  – 0.7x transistor dimension scaling every two years
  – Hi-K MG & Tri-Gate devices: significant energy-efficiency benefits

• Key challenges for Sub-22nm 1-100TOPS/Watt SOC platforms
  – Special-purpose accelerators for graphics/video/media DSP
  – Ultra-low-voltage/NTV operation with wide dynamic voltage range
  – On-die reconfigurable logic fabrics/accelerators for flexible SOCs

• Energy-efficient SOC graphics/media processing:
  – Reconfigurable SIMD vector permutation processor in 22nm
  – NTV processor with wide dynamic range in 32nm CMOS
  – Fine-grain reconfigurable logic array fabric in 32nm CMOS

• Ultra-low voltage (NTV) circuit design challenges & opportunities
  – 5-10X higher energy efficiency (GOPS/W) vs. nominal supply operation
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