Extending Modular Redundancy to NTV: Costs and Limits of Resiliency at Reduced Supply Voltage

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Agenda

• Pros and Cons of Near-Threshold Computing (NTC)
• Towards the Goal of Simultaneous Increase in Resilience and Energy Efficiency
• Impact of Performance Variability for N-MR Systems
• Experimental Setup
• Energy Cost of Mitigating Variability
• Conclusions and Future Work
Increasing Interest in Near-Threshold Computing: Limits

- **Voltage Scaling** is a very effective way to reduce energy consumption
  - Total Energy = $E_{\text{dynamic}} + E_{\text{static}}$
  - Dynamic Energy directly proportional to $V_{\text{DD}}^2$
  - $E_{\text{static}}$ proportional to ($V_{\text{DD}} \times \text{Leakage current} \times T_{\text{clk}}$)

- Extreme reduction of $V_{\text{DD}}$
  - Sub-threshold region
  - Theoretical Lower Limit of $V_{\text{DD}}$ is 36 mV [1]
  - $\geq 12X$ Energy Savings as compared to Nominal
  - Massive Performance Penalty (exponential)
  - Limited Applicability


Increasing Interest in Near-Threshold Computing: In-Practice

- **Voltage Scaling** is a very effective way to reduce energy consumption
  - Total Energy = $E_{\text{dynamic}} + E_{\text{static}}$
  - Dynamic Energy directly proportional to $V_{\text{DD}}^2$
  - $E_{\text{static}}$ proportional to ($V_{\text{DD}} \times \text{Leakage current} \times T_{\text{clk}}$)

- Optimum reduction of $V_{\text{DD}}$
  - Near-Threshold region
  - Lower limit of $V_{\text{DD}}$ in commercial applications is \( \sim 70\% \) of nominal [1]
  - Only 2X Energy Difference from Sub-Threshold
  - 10X Delay Difference from Sub-Threshold
  - Still $> 6X$ Energy Reduction as compared to Nominal

Limitations of NTC: Soft Errors

- Soft Errors in logic datapath
  - Cause: Radiation-induced transient charge within a logic path which is ultimately latched by a F/F
  - More-than-ECC (Error Correcting Codes) needs to be done to mitigate soft errors for logic

- Soft Error Rate (SER) for logic at NTV is shown experimentally to be comparable to the SER for memory circuits [2]
  - Critical charge $Q_{\text{crit}}$ needed to cause a failure decreases as $V_{\text{DD}}$ is scaled. The SER has an exponential dependence on critical charge.
  - For 40nm and 28nm nodes, SER doubles when $V_{\text{DD}}$ is decreased from 0.7V to 0.5V

- Soft Error masking mechanisms for logic paths
  - Logical Masking: fewer gate in critical path to regain lost throughput, less chance of the pulse being masked by logical computation of other gates in the path.
  - Electrical Masking: large pulse transients are created, as compared to supply voltage
  - Latching-window masking: lowered operating frequency has positive impacts here

- Non-planar devices offer a means to reduce SER.
  - 22nm Tri-gate technology is shown to reduce neutron and alpha particle induced SER at nominal voltage by 4-fold and 10-fold respectively compared to a 32nm planar process [3]

- Reduced pipeline depths, technology scaling, and NTV can be anticipated to have detrimental effects on logic SER

Adoption of NTC for Embedded applications

- A new direction for highly-reliable energy-efficient Embedded Processors/Chips
  - Energy-Efficiency $\rightarrow$ NTC
  - High-Reliability $\rightarrow$ Spatial/Temporal Redundancy

- Spatial Redundancy used in mission-critical applications for resilience as spare components help to tolerate failures [4],[5]
  - Harsh environments: autonomous vehicles, satellites, etc.
  - It is possible to reduce overhead by protecting only the critical components

- Temporal Redundancy (Repeated Execution) is also effective for soft error masking, however, performance loss is massive.
  - Suitable for area-constrained applications

- Spatial: $N$-Modular Redundancy ($N$-MR) and majority voting
  - System operates correctly as long as majority of the modules are functioning
  - Typically, $N=3$ is employed: referred to as TMR systems
Soft Error Masking at NTV

- SER in logic paths can be reduced by schemes such as gate-sizing [6] and dual-domain supply voltage assignment [7]
  - Harden components which are more susceptible to soft errors. For instance, logic gates near the flip-flop
  - Difficult to provide comprehensive coverage. For instance, dual-domain voltage assignment is only able to reduce SER by 33.45%
- TMR provides comprehensive masking against soft-errors
  - Most soft-errors are mask-able or diagnosable
  - The probability of a non-diagnosable error is very low, i.e. what is the probability of majority instances producing identical and invalid outputs?
  - Temporal or Spatial Multiple Bit-Upset (MBU) should generate (with high probability) a diagnosable error

Related Work: Impact on Commercial Systems

- Variable Strength ECCs have been employed for reliable cache operation under aggressive voltage scaling [8]
- For processor caches operating at NTV, TMR is employed as a low-complexity means for improved resilience as compared to ECC schemes [9]
- Employing Modular Redundancy for High-Performance Computing (HPC) systems can significantly increase compute node availability [C. Engelmann et al. 2009]
  - HPC systems: decreasing MTTF, increasing MTTR due to scaling
  - Checkpoint and Restart is too costly (for complex HPC applications, increasing volume of state information needs to be saved)
  - Employing compute-node (processor(s), memory module(s), network interface) level redundancy permits to tradeoff individual component reliability by a factor of 100-100,000 → $Less Expensive$
Limitations of NTC: Process Variations

- Near-Threshold Computing provides Energy-Efficiency
  - >10X Performance Loss → Parallelization [11], Device optimization [1]
  - (add-on) 5X Impact of Performance Variation → Cost of Design Margins?
- Nanoscale CMOS devices have Performance variability caused due to manufacturing-induced Process Variations (PV) [12].
  - For example, Random Dopant Fluctuations (RDF) are due to implanted impurity fluctuation and cause local variation (intra-die) in the threshold voltage of the transistors → Increase in Delay Margins
  - Impact of Technology Scaling: RDF magnified as number of dopant atoms is fewer so addition or deletion of just a few impurity atoms significantly alters transistor properties
- Operation near the threshold voltage of the transistors further exacerbates the process variability [1],[13]

Limitations of NTC: Delay Variations

- Delay measurements of FO4 Inverter Chains
- Implemented using PTM cards

![Graph showing variation 3σ/μ (%)](attachment:image)
Module Redundancy at NTV:
What is the catch?

Module # 1
[Delay 4.5ns]

Module # 2
[Delay 6ns]

Module # 3
[Delay 5.5ns]

Majority Voter
[0.5ns]

Need to consider the worst delay out of all N modules

\[ \tau_{NMR} = \max_{1 \leq i \leq N} (\tau_i) + \delta \]

Clock = (1/6.5ns)

N-MR system Delay Distributions under PV

Delay Distributions (1000 arrangements each) at NTV of 0.55V with 45nm PTM model cards

Increasing N →
Performance of $N$-MR systems with scaled technology nodes

Mean delay difference of $N$-MR systems increases with voltage scaling down to Near-threshold region

![Graph showing mean delay difference vs voltage for different technology nodes and $N$ values.](image)

$N=3, 5$

Increasing $N$ → $\mu \uparrow$

The effect is more prominent here

Performance of $N$-MR systems and variability

Delay Variations decrease with increasing $N$ for $N$-MR systems

![Graph showing delay variation vs voltage for different technology nodes and $N$ values.](image)

$N=3, 5$

Increasing $N$ → $\sigma \downarrow$
Reducing variability at NTV

• Variability is dependent on length of the critical path. More gates imply less variability [14]

• Type of logic gate utilized can impact variability

Functionally equivalent, yet physically diverse chains exhibit different variability

Reducing variability at NTV

• Develop a synthesis technique which realizes same function utilizing different gates with the goal of minimizing variability within given constraints

TMR systems based on NAND gate exhibit the least amount of variability
Future work: synthesizing variability immune circuit for NTV operation

• For our experiments with the inverter chains, the mean delays for NAND-based systems are higher than INV-based systems which outweighs any benefit of reduced variation.

Energy Cost of Mitigating Variability

• “One-Time” Timing Guard-bands
  • Voltage and/or Frequency Margin [15]

• For a fixed $V_{DD}$ of simplex system, how much voltage margin ($\Delta V_{DD}$) needs to be added for $N$-MR system?
  • Left-shift the distribution of NMR system towards that of the simplex system

• Condition for same 99% Yield for $N$-MR system as compared to simplex system i.e., same delay [14]
  • (for $N \geq 3$): $\mu_{N-MR} + 3*\sigma_{N-MR} \leq \mu_{Simplex} + 3*\sigma_{Simplex}$

• How much energy overhead for $N$-MR system?
  • N-fold as mostly assumed with $N$-MR systems
**Experimental Setup**

- MCNC benchmark circuits c880, i5
- 45nm-based NanGate open source library [16]
- Synopsys Design Compiler used for synthesis
- Worst-case Test Vectors are generated using Synopsys TetraMax
- Synthesized netlists are imported into HSPICE for Monte-Carlo simulations
- Voter delay is not considered to make direct comparison to simplex systems

![Image](http://images.dailytech.com/nimage/22944_large_2007_08_monte_carlo.jpg)

**Experimental Setup**

- At least 1000 Monte-Carlo iterations are performed
- $\mu V_{th}$ from Predictive Technology Model (PTM) cards
- RDF: $\sigma V_{th}$ ranges from 25.9mV (45nm) to 59.9mV (22nm) [12]
Results: Energy-Efficiency vs Reliability

- Energy measurements of FO4 Inverter Chains implemented using 45nm PTM cards

<table>
<thead>
<tr>
<th>Operating Point</th>
<th>$V_{dd}$ (V)</th>
<th>Normalized Energy</th>
<th>Normalized Delay</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>1.1</td>
<td>1X</td>
<td>1X</td>
</tr>
<tr>
<td>B</td>
<td>0.69</td>
<td>~1X</td>
<td>2.58X</td>
</tr>
<tr>
<td>C</td>
<td>0.545</td>
<td>~1.01X</td>
<td>7.15X</td>
</tr>
</tbody>
</table>

Energy Consumption of $N$-MR systems

- How much Voltage Margin (VM) expressed as $\Delta V_{dd}$ needs to be included for $N$-MR system?
- Even though $N$-MR systems exhibit higher mean delays, the reduced variance necessitates only a slight VM to meet the delay target of the simplex system
- On average 2mV increase in $V_{dd}$ is satisfactory to operate a TMR arrangement based on i5 circuit at comparable delay

<table>
<thead>
<tr>
<th>Benchmark →</th>
<th>c880</th>
<th>i5</th>
</tr>
</thead>
<tbody>
<tr>
<td>Simplex, $V_{dd}$ (NTV)</td>
<td>N=3</td>
<td>N=5</td>
</tr>
<tr>
<td>0.55 V</td>
<td>3.03X</td>
<td>5.06X</td>
</tr>
<tr>
<td>0.6 V</td>
<td>3.03X</td>
<td>5.05X</td>
</tr>
<tr>
<td>0.65 V</td>
<td>3.02X</td>
<td>5.04X</td>
</tr>
<tr>
<td>0.7 V</td>
<td>3.01X</td>
<td>5.03X</td>
</tr>
</tbody>
</table>
Results of VM: Increased Variability

- The mean delays for the 22nm (45nm) node with N = 3 & N = 5 are 1.16X (1.06X) and 1.24X (1.09X) the mean delay for a simplex system respectively at the same voltage of 0.55V
- The 22nm node-based 5MR system requires 3.94% more energy consumption than a similar configuration at 45nm
- At NTV of 0.5V for simplex arrangement, a 11mV increase in V_{DD} is required for the TMR arrangement for same performance

<table>
<thead>
<tr>
<th>Technology Node →</th>
<th>45nm</th>
<th>22nm</th>
</tr>
</thead>
<tbody>
<tr>
<td>simplex, V_{DD} (NTV)</td>
<td>N=3</td>
<td>N=5</td>
</tr>
<tr>
<td>0.5 V</td>
<td>3.04X</td>
<td>5.07X</td>
</tr>
<tr>
<td>0.55 V</td>
<td>3.03X</td>
<td>5.05X</td>
</tr>
<tr>
<td>0.6 V</td>
<td>3.03X</td>
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<tr>
<td>0.65 V</td>
<td>3.02X</td>
<td>5.03X</td>
</tr>
<tr>
<td>0.7 V</td>
<td>3.01X</td>
<td>5.02X</td>
</tr>
</tbody>
</table>

Conclusions and Future Work

- Redundancy provides a degree of freedom for increased reliability by diminishing the supply voltage
- Feasible when resulting increase in delay is tolerable
- Further study worthwhile to determine resilience provided by N-MR systems at NTV due to other noise sources such as:
  - Variation in supply voltage V_{DD} and Temperature
    - Expect a further variation of 2X [1] (detrimental effect anticipated)
  - Aging-induced variations [13]
    - Lower Voltage and Junction temperatures will lower aging effects such as Bias-Temperature Instability (beneficial effect anticipated)
    - Lower temperature and currents help to reduce interconnect defects due to Electromigration (beneficial effect anticipated)
References (1/2)


References (2/2)


