Using STT-RAM to Enable Energy-Efficient Near-Threshold Chip Multiprocessors

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Near-Threshold CMP Design Challenges

**Problem:** Increasing core counts in CMPs → “Power Wall” → “Dark Silicon”

**Solution:** Near-Threshold Computing

**Challenges:**
1. performance degradation;
2. amplified process variation;
3. leakage power dominates.

Leakage power dominates in NT-region

Cache power is mainly leakage dominated

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STT-RAM Based NT-CMP Design

Key Ideas:

• Use STT-RAM for all caches:
  • STT-RAM @ High-Vdd, cores @ NT-Vdd → fast cache reads.
  • Clustered-CMP in which the L1 caches are shared within each cluster, removing coherence costs.

• Address variation-induced performance heterogeneity:
  • Shared L1 cache enables low overhead within-cluster thread migration.
  • Periodically migrating threads between “fast” and “slow” cores achieves homogeneous CMP performance.

Proposed design reduces power consumption by 7%, improves performance by 17%, and reduces energy by 21%.