



Circuit Reliability: Mechanisms, Monitors, and Effects in Near-Threshold Processors

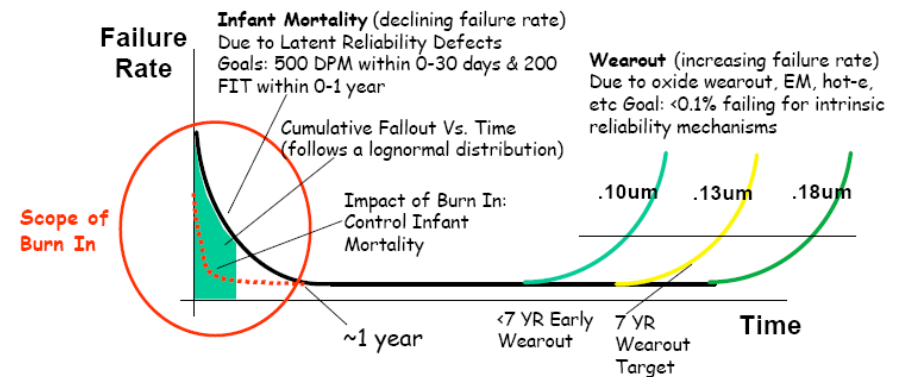
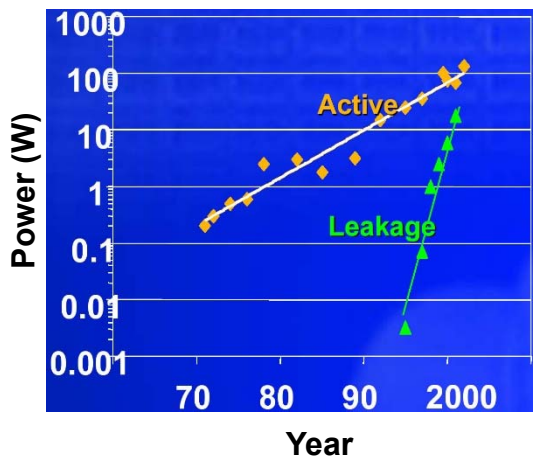
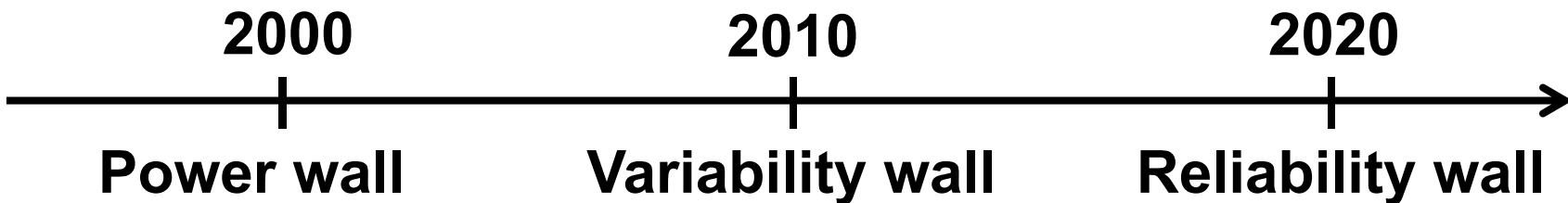
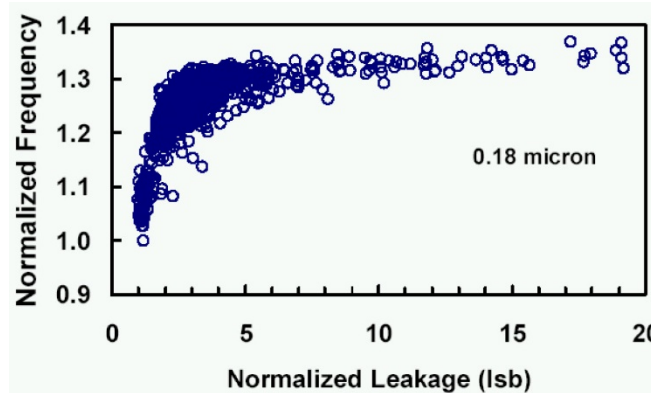
Chris H. Kim

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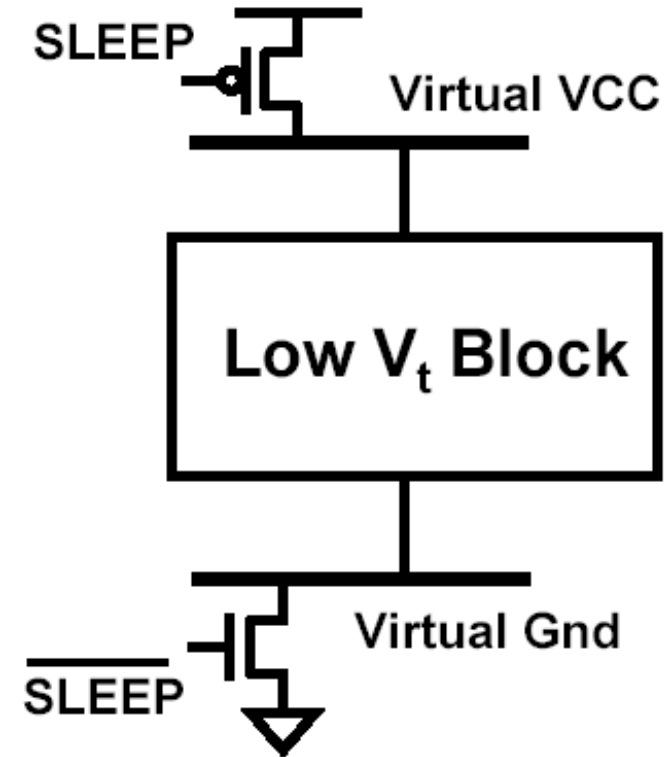
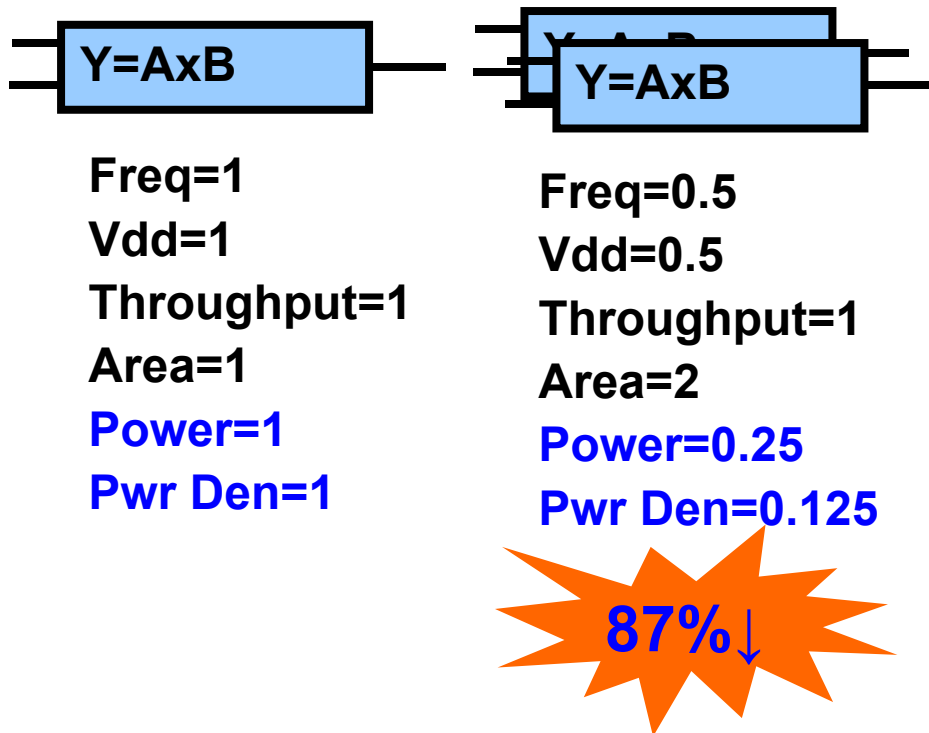
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Scaling Challenges

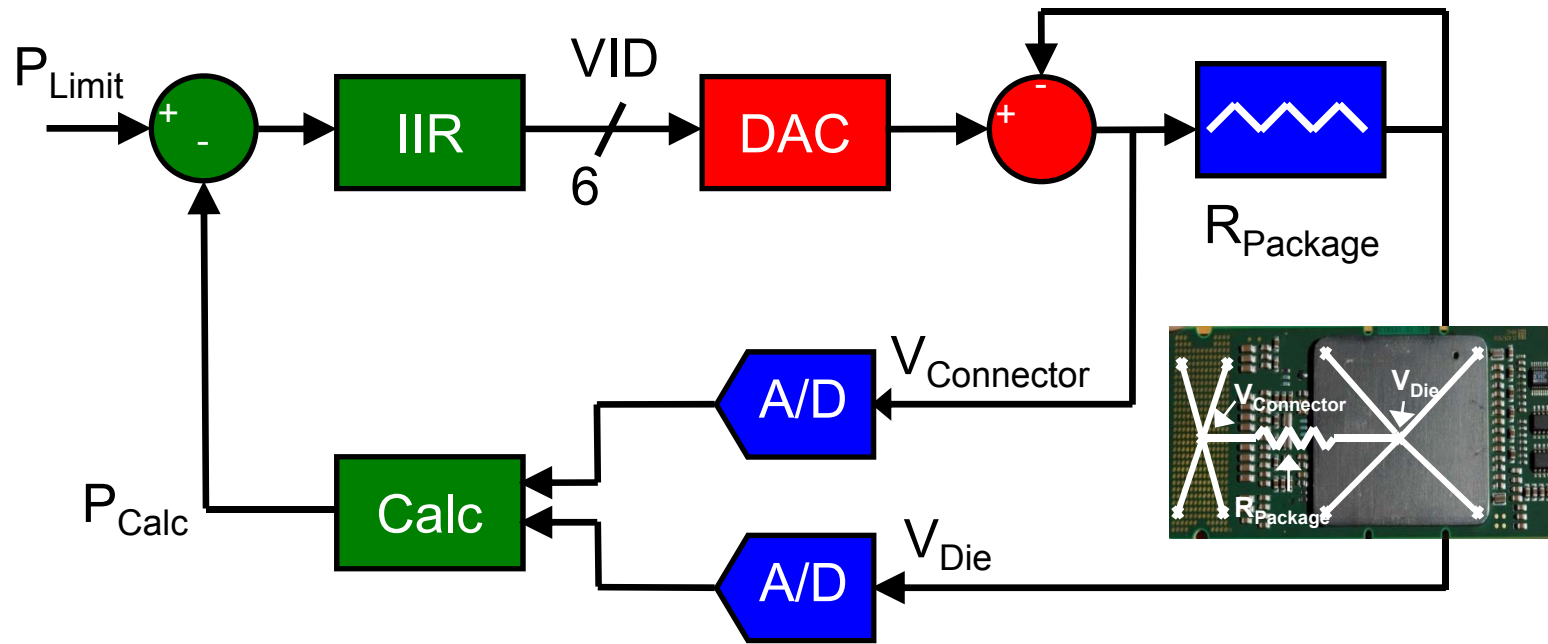


Overcoming the Power Wall



- Proven solutions: Multi-core chips, dynamic voltage frequency scaling, clock gating, power gating, ...

Overcoming the Variability Wall



Micro-Controller

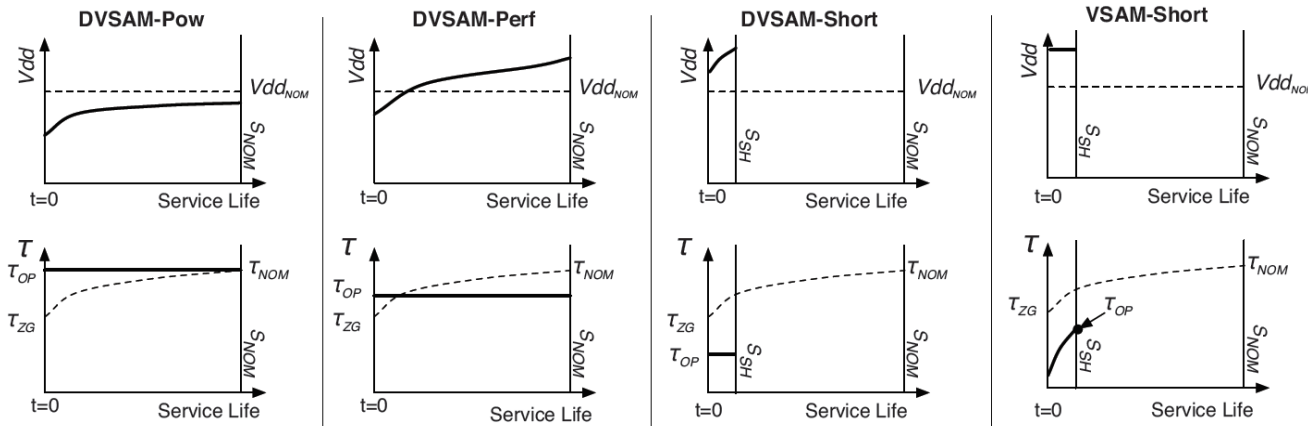
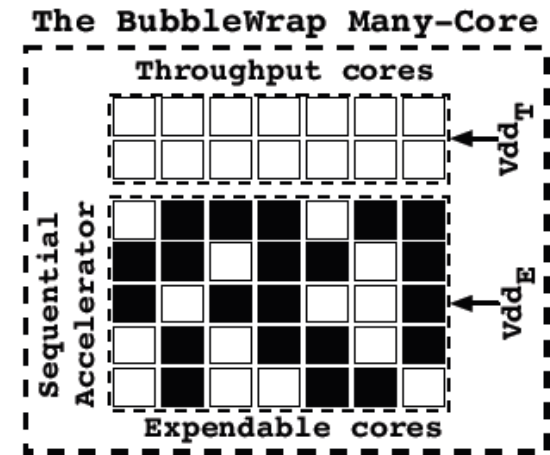
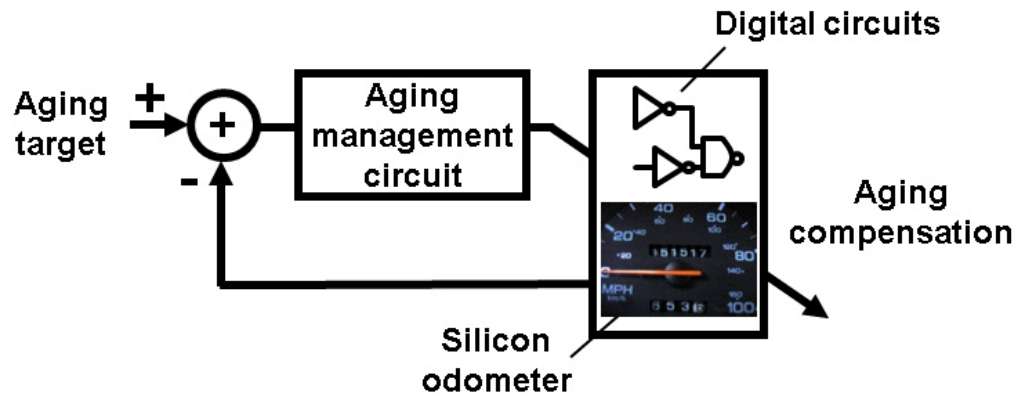
Power Supply

Package/Die

Intel Foxtan Technology

- **Proven solutions: Variation aware design, memory assist/repair, lithography techniques, adaptive systems**

Overcoming the Reliability Wall

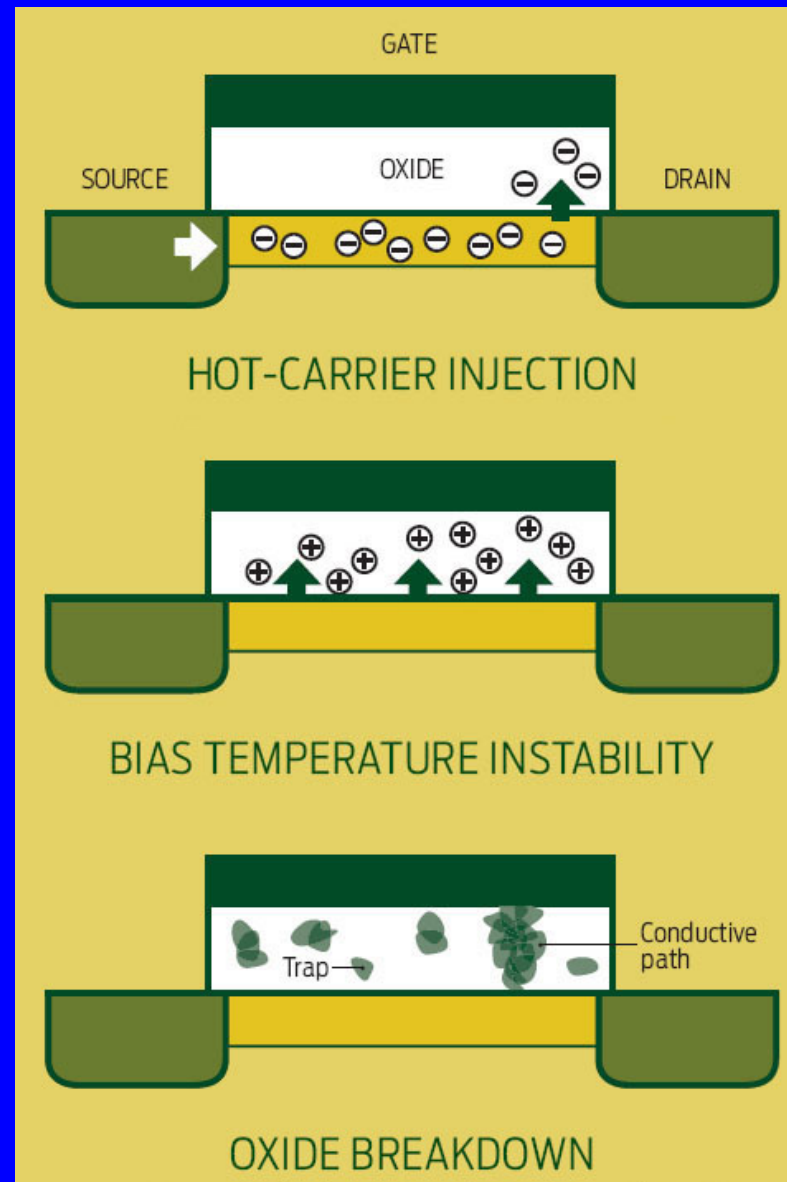


- Possible solutions: Guardbanding, sensing and compensation, wear-leveling, failure resistant systems, ...

Outline

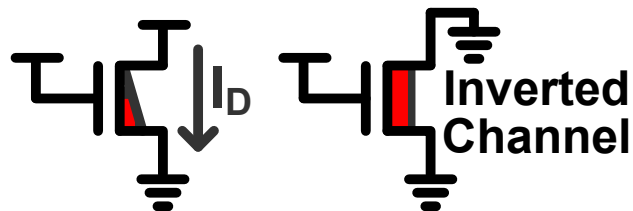
- **Device Reliability Issues**
- Reliability Monitors and Measurements
- Reliability Effects in NTV Processors
- Summary

Aging in CMOS Transistors



HCI, BTI, and TDDDB in Digital Logic

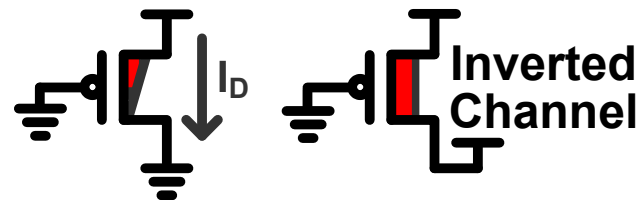
NMOS



HCI

PBTI, TDDDB

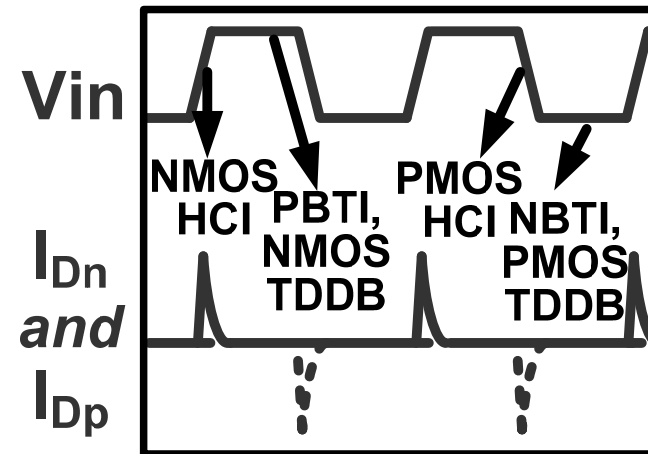
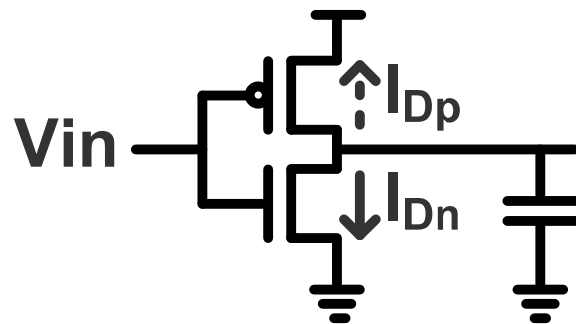
PMOS



HCI

NBTI, TDDDB

Inverter

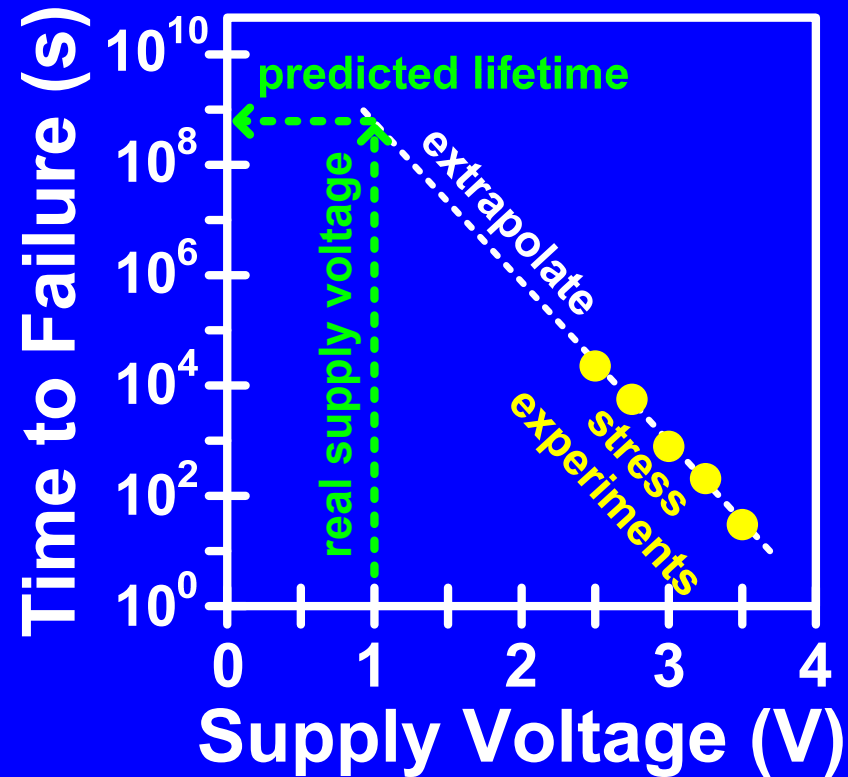


- Transistors are exposed to different stress conditions during normal digital circuit operation

Practical Solutions for Preventing Aging Related Failures

- **BTI and HCI**
 - Gradual decline in performance
 - Guard banding (static or dynamic), adjust V_{max}
 - CAD, firmware & architecture level support essential
- **TDDB**
 - Single incident may lead to outright system failure
 - Can happen anywhere inside a chip
 - Improve fabrication procedure, adjust V_{max}
- **Bottom line: Precise measurement and understanding of circuit degradation a key aspect of robust design**

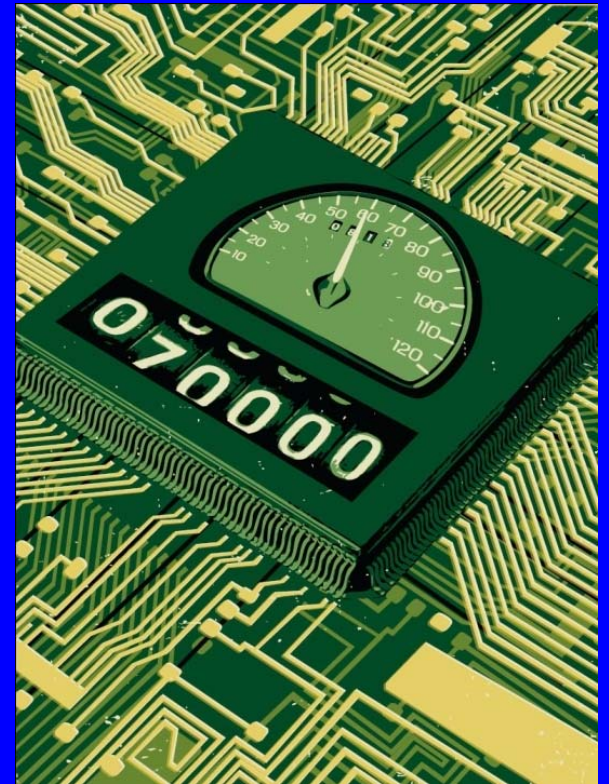
Transistor Lifetime Estimation



- **Extrapolate stress results with respect to:**
 - Op. conditions based on acceleration models
 - Larger chip areas (e.g., Poisson scaling for TDDB)
 - Lower percentiles based on chosen distribution

Benefits of In-Situ Reliability Monitors over Device Probing

- Information from actual circuits (test circuit must be representative)
- High (timing) precision + short measurement interrupt
- No expensive equipment
- Short test time and reduced test area
- Measurements at use condition → allows realistic lifetime projection
- Complements traditional probing methods



Usage Scenarios and Design Issues of In-situ Reliability Monitors

- **Usage scenario 1: Process characterization and yield improvement**
 - Early technology characterization is often performed before many metallization layers are being fabricated
 - Library cells may not be available (flip-flops, scan)
 - Device probing would still be a competitive solution for extracting analog parameters such as I–V or C–V
- **Usage scenario 2: In-field monitoring and data collection**
 - Workload unknown
 - Simple circuits are practical but they have limited capabilities
 - Firmware and architecture support needed

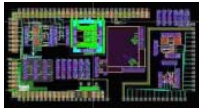
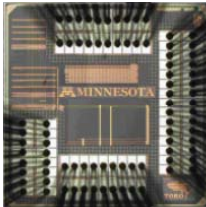
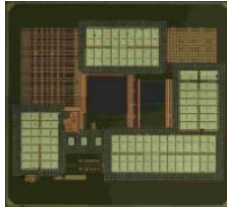
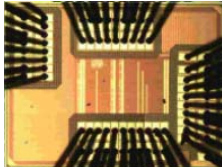
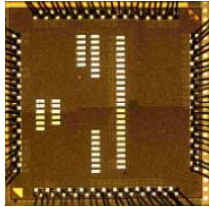
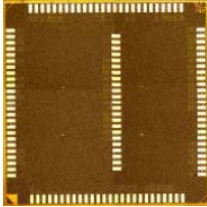
Usage Scenarios and Design Issues of In-situ Reliability Monitors

- Usage scenario 3: Sensor for real time aging compensation
 - Effectiveness versus overhead
 - Measurements are from a proxy circuit
 - Practical issues: type of sensor, temporal granularity, spatial granularity, communication with sensors, interface and protocol
 - Personally not a big fan

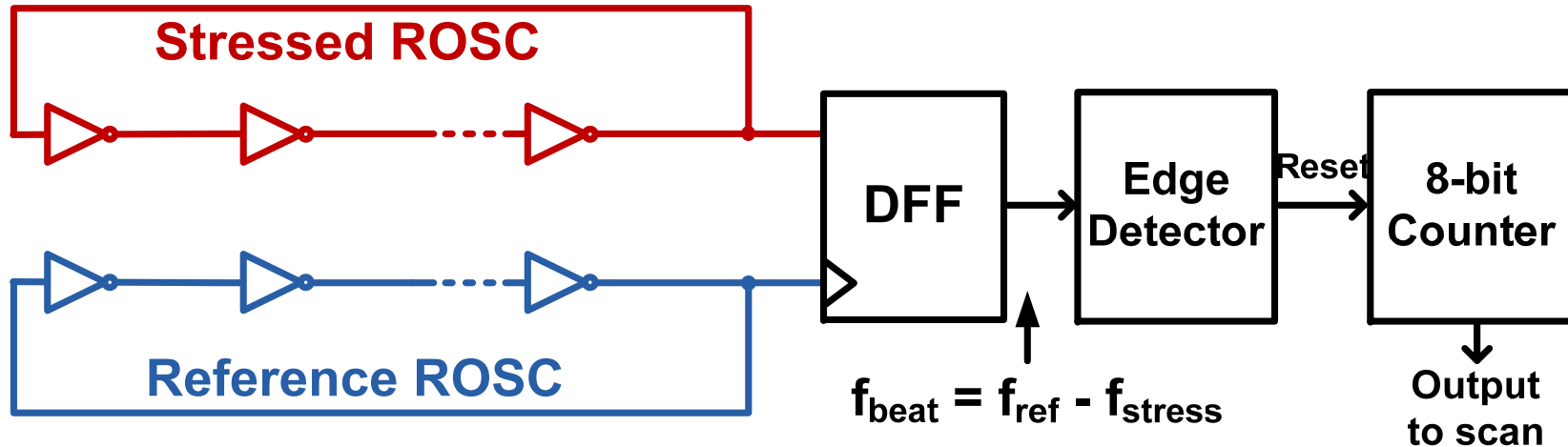
Outline

- Device Reliability Issues
- **Monitors and Measurements**
- Effects in NTV Processors
- Summary

Circuit Based Reliability Monitors (or Silicon Odometers)

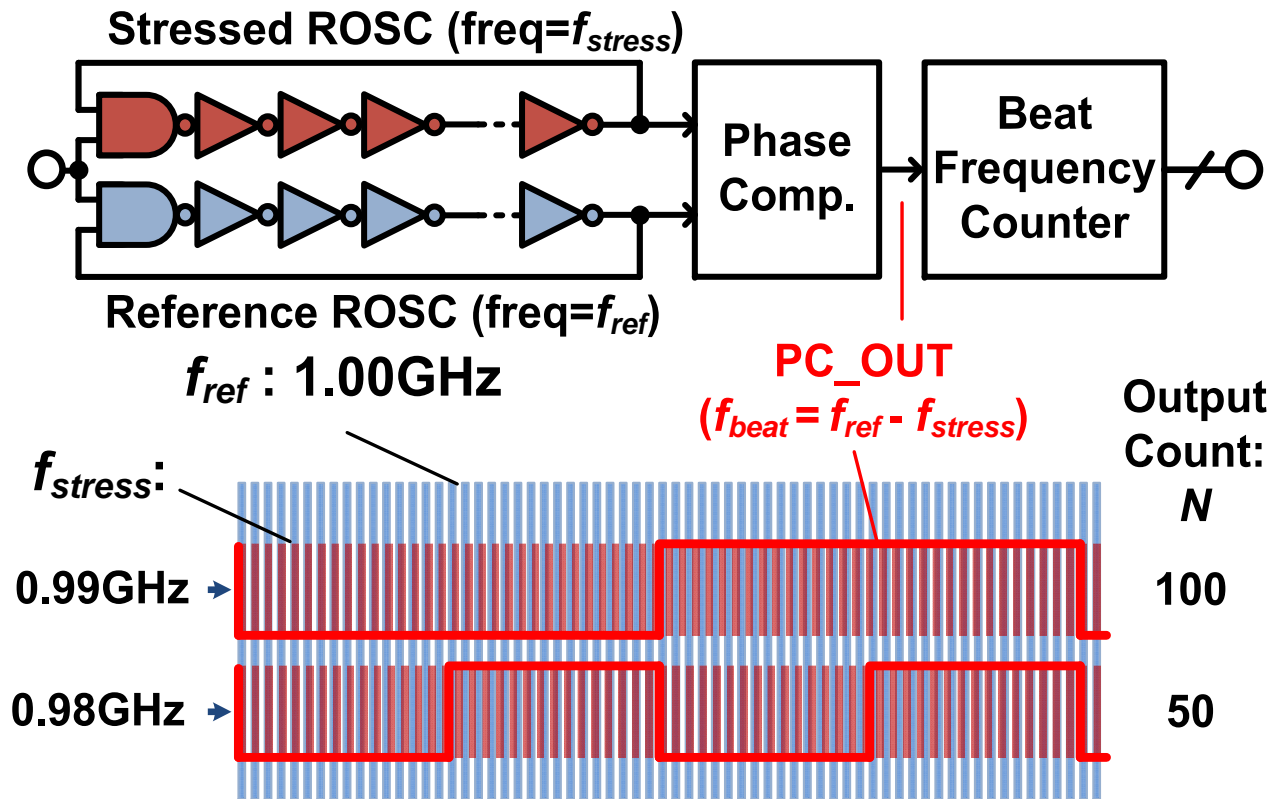
Year	2007	2008	2009	2010	2011	2012
Die Photo						
Process	130nm	65nm	65nm	65nm	32nmSOI	32nmSOI
Odometer Projects	Original Silicon Odometer	All-In-One Odometer	Statistical, Duty-Cycle, and RTN Odometer	Interconnect Odometer	PBTI and SRAM Odometer	SRAM and RTN Odometer
Focused Reliability Issues	NBTI Induced Frequency Degradation	Separately Monitoring NBTI, HCI and TDDB	Statistical Behavior of NBTI; RTN on Logic Circuit	Impact of Interconnect on BTI and HCI Aging	Monitoring PBTI in HKMG Process; BTI Impact on SRAM Read/Write	SRAM Timing Issues Due to BTI; RTN Impact on Ring Oscillator

Beat Frequency Silicon Odometer



- **Beat frequency of two free running ROSCs measured by DFF and edge detector**
- **Benefits of beat frequency detection system**
 - Achieve ps resolution with μs measurement interrupt
 - Insensitive to common mode noise such as temperature drifts
 - Fully digital, scan based interface, easy to implement

Beat Frequency Silicon Odometer



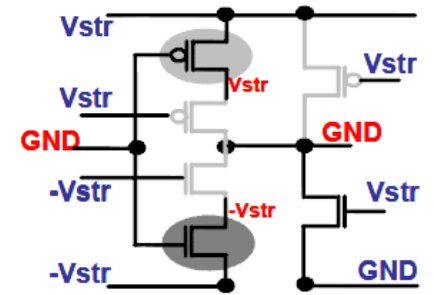
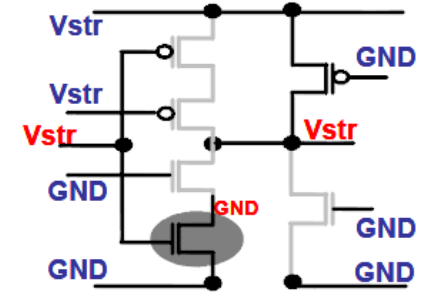
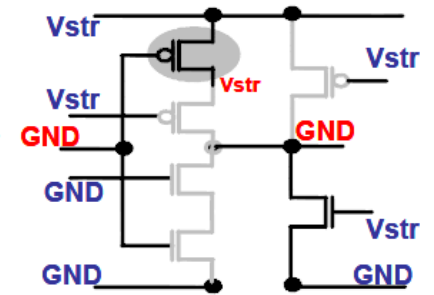
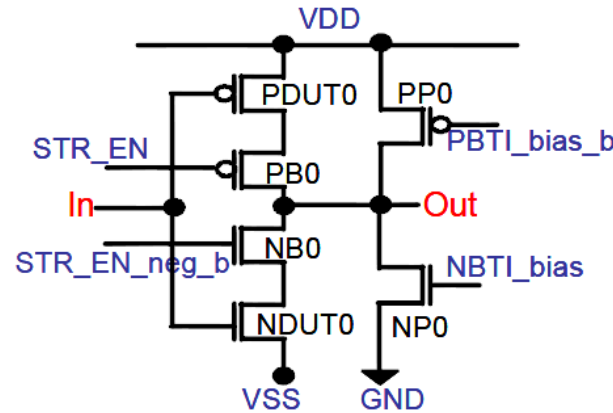
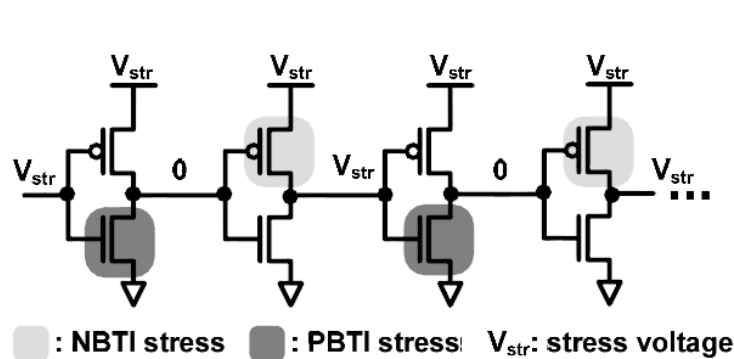
- **Sample stressed ROSC output with reference ROSC**
 - 1% frequency difference before stress $\rightarrow N=100$
 - 2% frequency difference after stress $\rightarrow N=50$
 - Δf or ΔT sensing resolution is $>0.01\%$

ROSC Based Aging Sensor Comparison

System	Single ROSC	2 ROSC, simple	2 ROSC, beat freq.
Block Diagram			
Function	Count Stress ROSC periods during externally controlled meas. time	Count Stress ROSC periods during N1 periods of Ref. ROSC	Count Ref. ROSC periods during one period of PC_OUT
Features	Simple; compact	Simple; immune to common mode variations	High resolution w/ short meas. time; immune to common mode variations
Issues	Voltage and temp. variations; meas. time vs. resolution tradeoff; requires absolute timing reference (e.g. oscilloscope)	Meas. time vs. resolution tradeoff	Requires extra circuits (e.g., Phase Comp., edge detector, etc...)
Meas. time for 0.01% max res. *	30 μ s	30 μ s	0.3 μ s
Meas. error wrt. common mode variations **	+10.18% / -8.57%	+0.26% / -0.38%	+0.06% / -0.07%

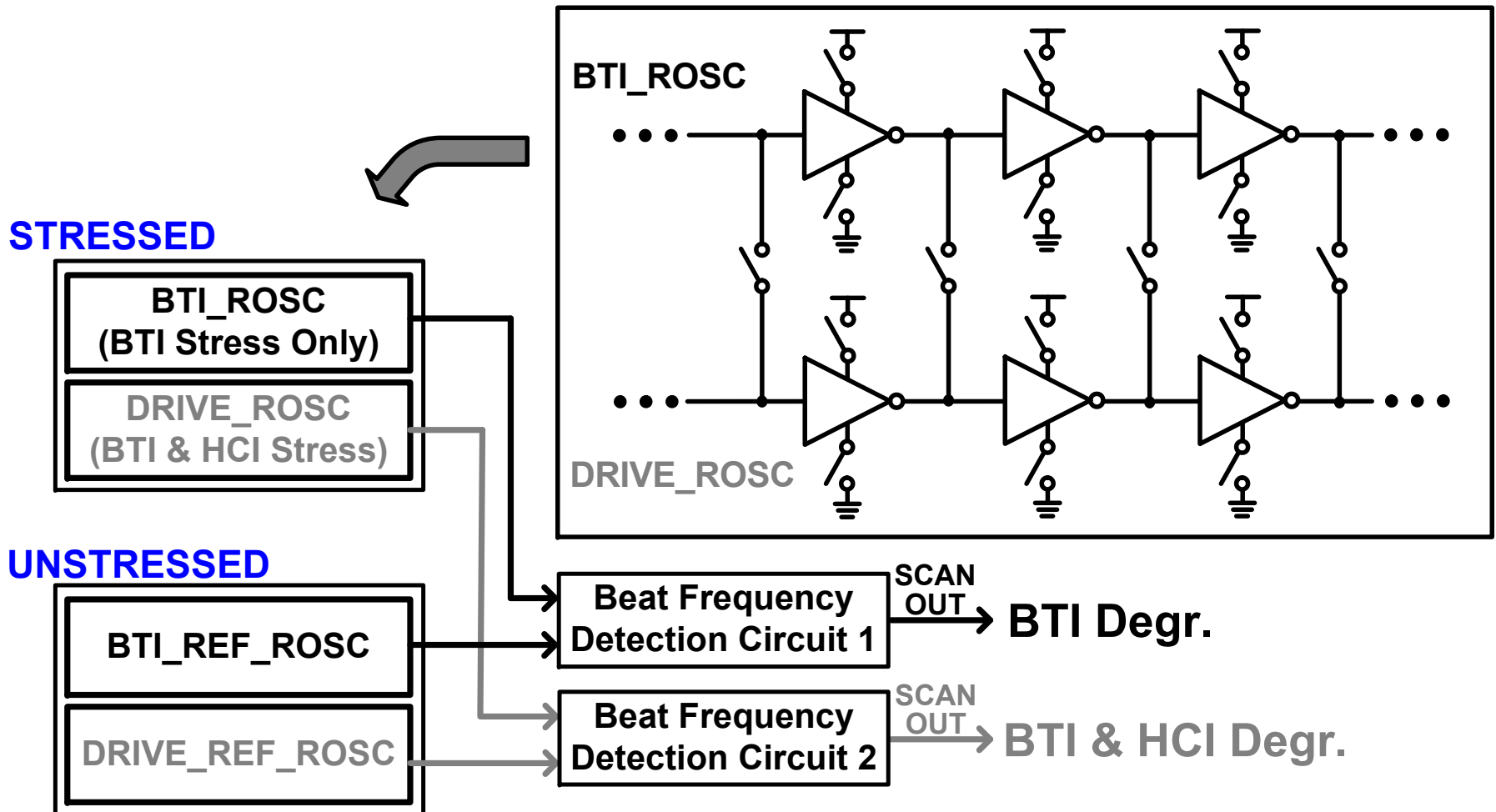
*ROSC period = 3 ns ** simulated with +/- 4% Δ VCC

Separately Monitoring NBTI and PBTI

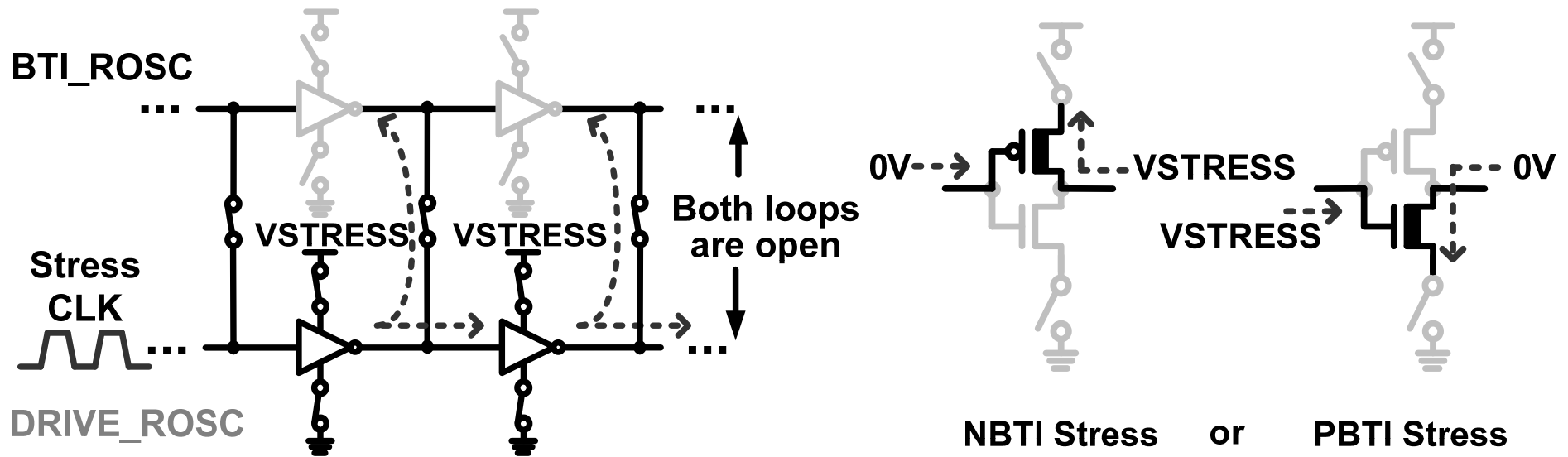


- PBTI becoming an important concern in high-k metal-gate
- Conventional Ring Oscillator (ROSC) can only provide overall frequency degradation information due to combined NBTI and PBTI effects
- New RO structure separates NBTI and PBTI effects

Separately Monitoring BTI and HCI

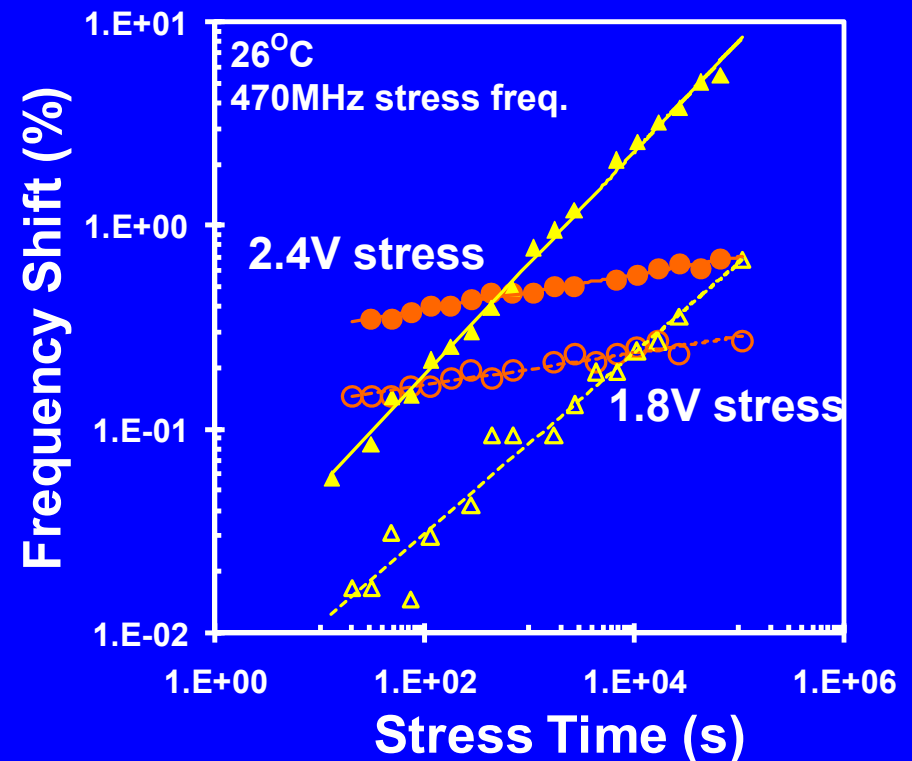
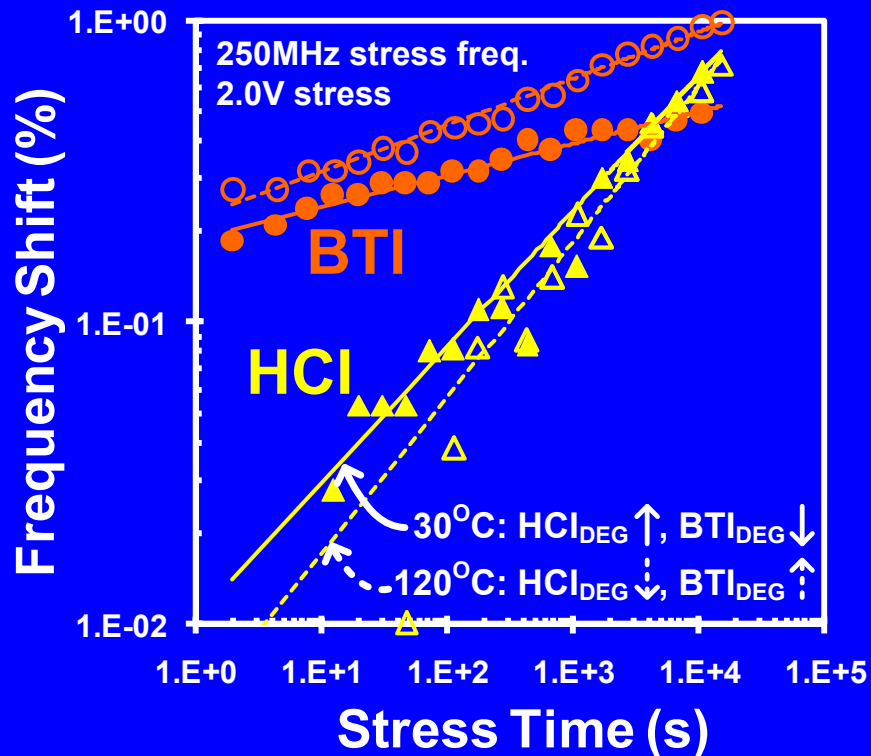


Separately Monitoring BTI and HCI



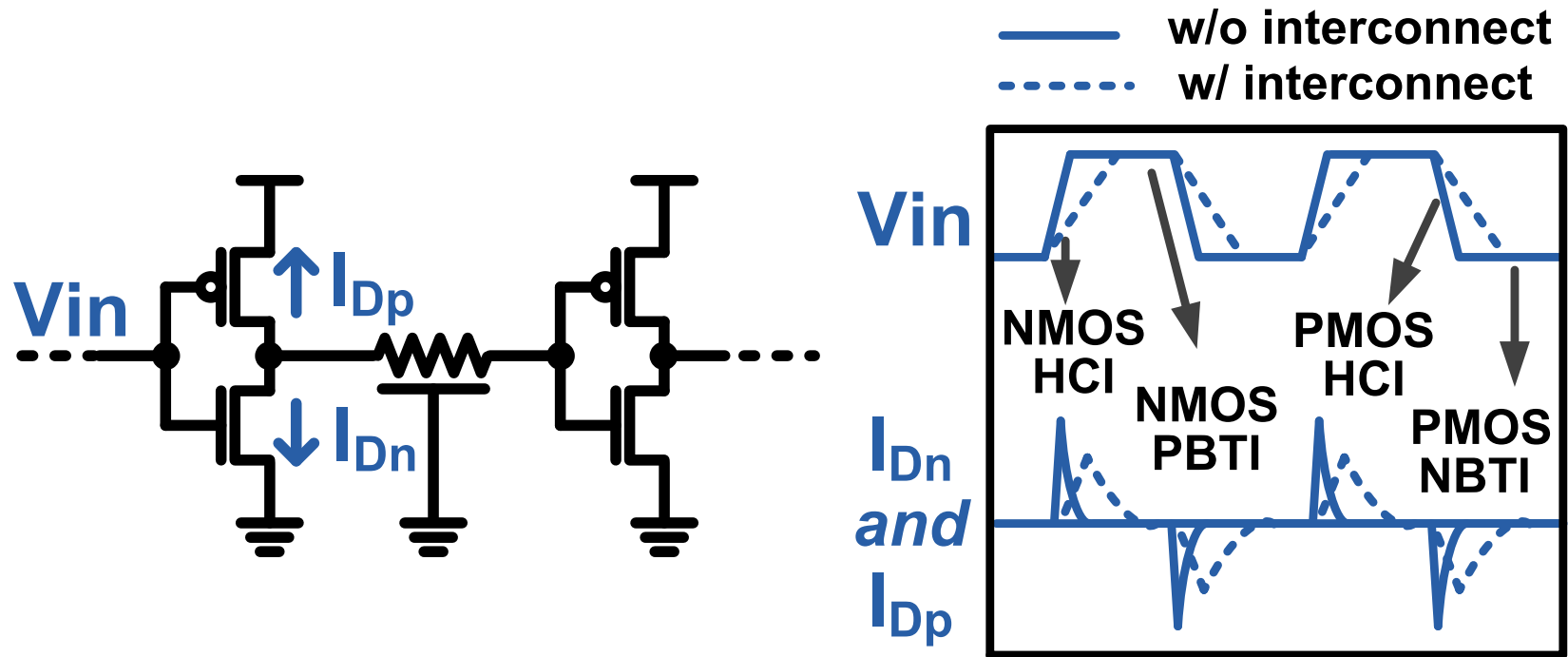
- Backdriving action equalizes BTI in both **BTI_ROSC** and **DRIVE_ROSC**
- Negligible HCI in **BTI_ROSC**: only 3-5% of the switching current in the **DRIVE_ROSC**
- Fresh power gates are used for frequency measurements

Temp. and Voltage Dependencies



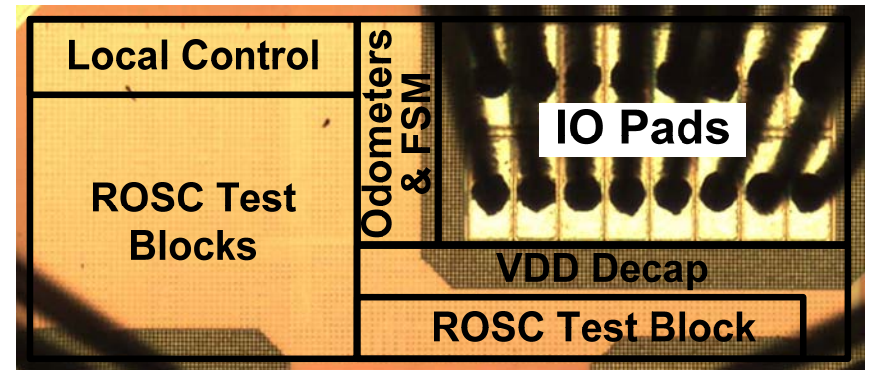
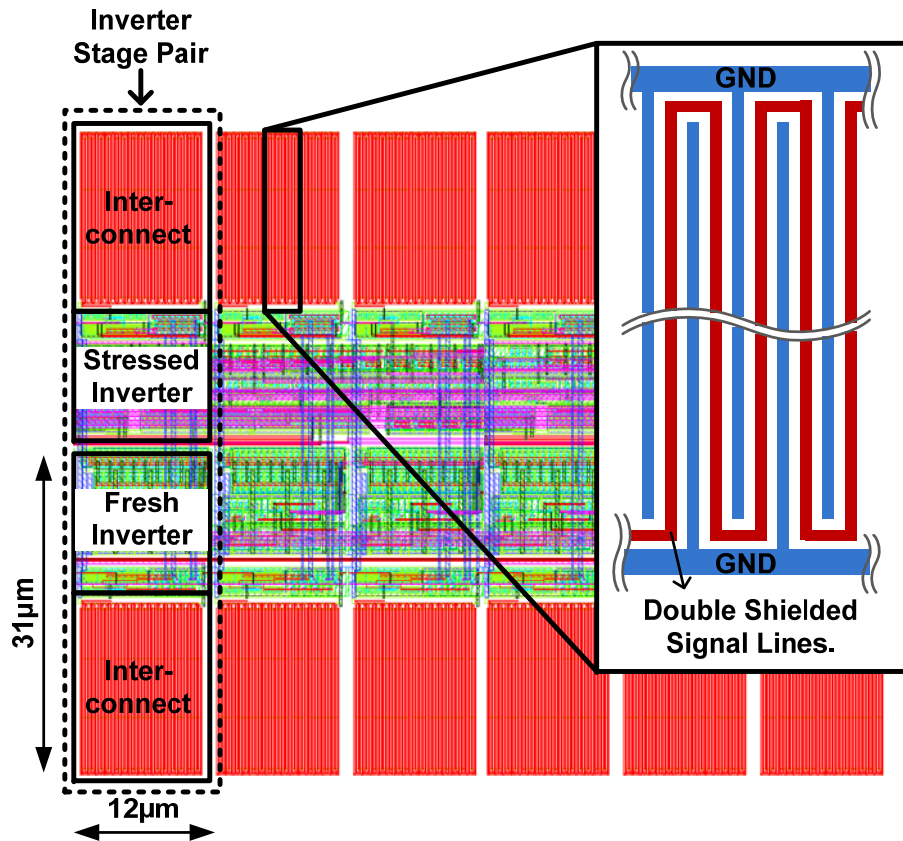
- HCI slightly reduced with temperature
 - Due to reduced drain current
- Both mechanisms degrade with stress voltage
 - Point when HCI begins to dominate pushed out in time by >1 order of magnitude at 1.8V vs. 2.4V

Aging Issues in Interconnects



- Interconnect affects the voltage and current shapes
 - Increased transition time (decreased slew rate)
 - Increased current pulse; decreased current peak value
- BTI and HCI have different sensitivities to bias conditions

Interconnect Aging Monitor



Process	65nm LP CMOS
Core / IO Supplies	1.2V / 2.5V
Stress Voltage	1.8V, 2.4V
Active Area	0.182mm ²
Interconnect Layer	M2, W=100nm, double shielded w/ 100nm spacing
Δf Resolution	> 0.016%
Meas. Interrupt	< 3µs

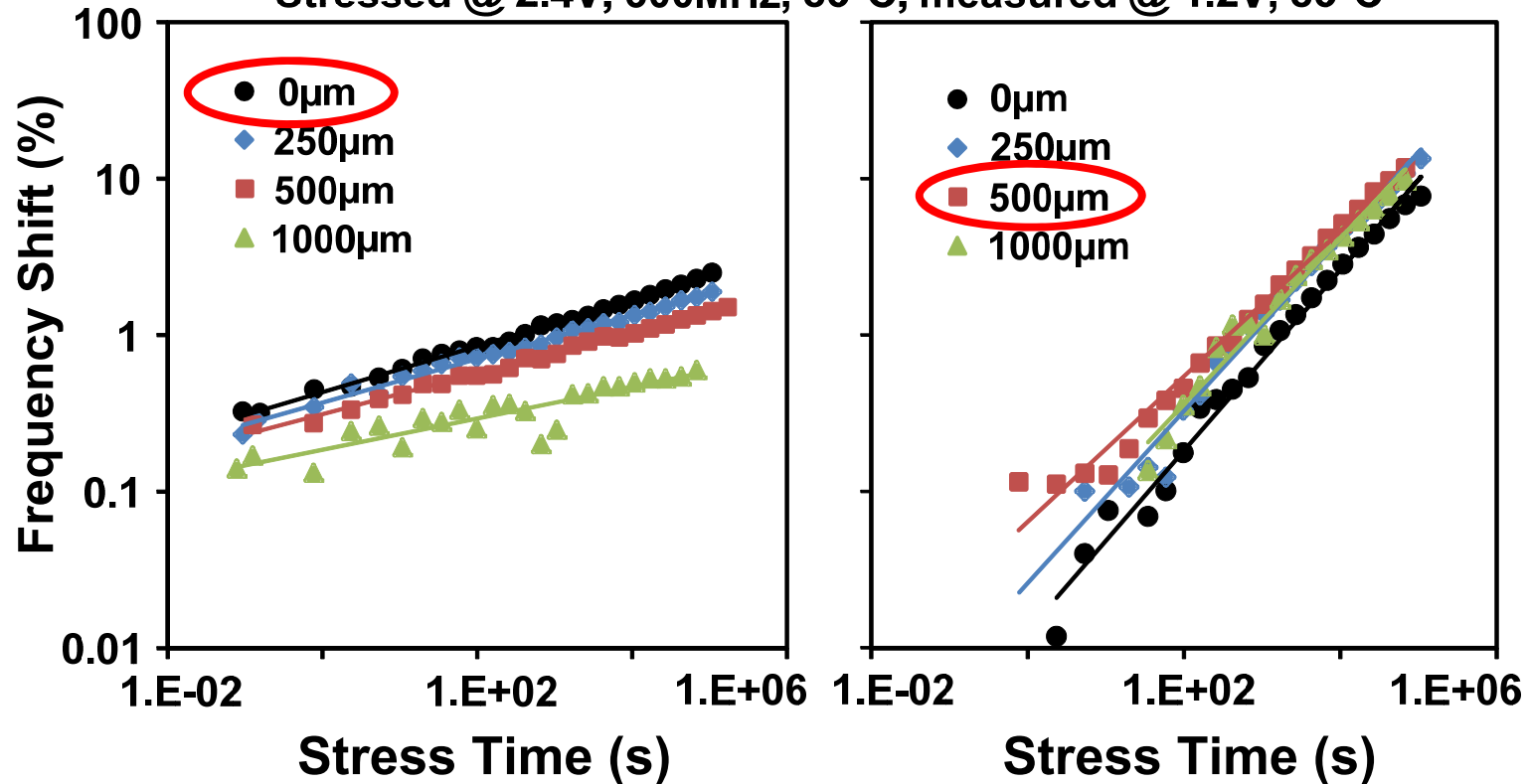
- **Serpentine wires for a dense chip implementation**
- **Ground shielding on both sides for reducing noise**

BTI and HCI Aging: With Interconnect

BTI aging

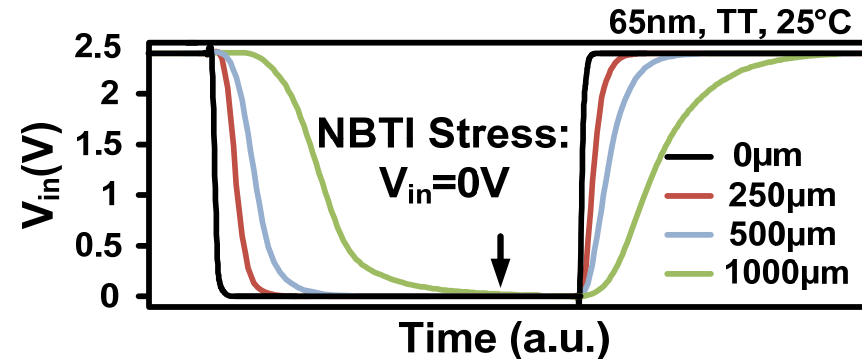
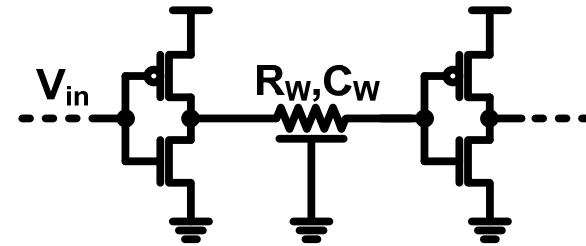
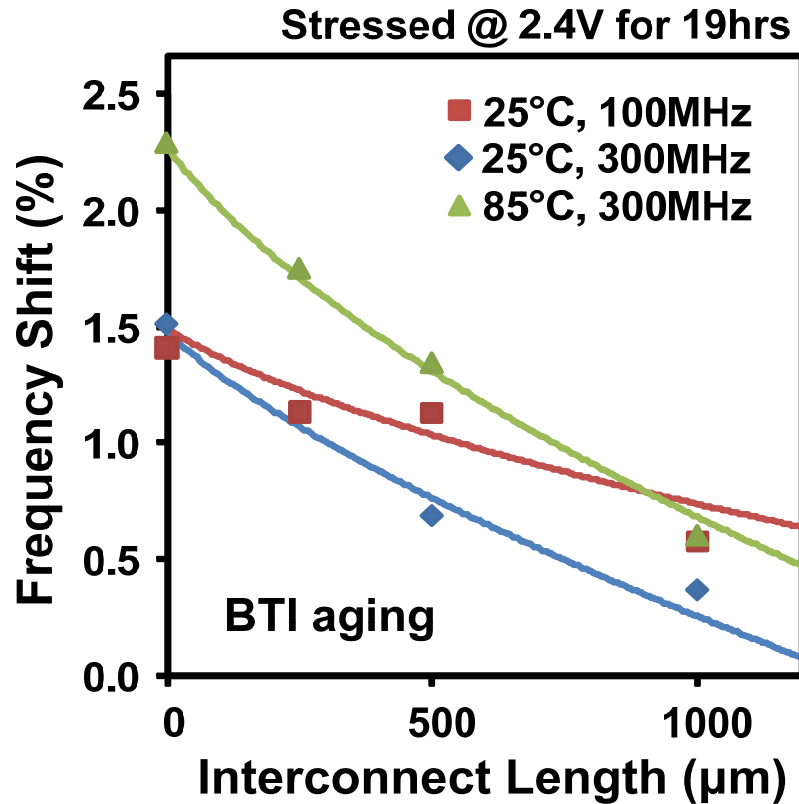
HCI aging

Stressed @ 2.4V, 300MHz, 85°C, measured @ 1.2V, 85°C



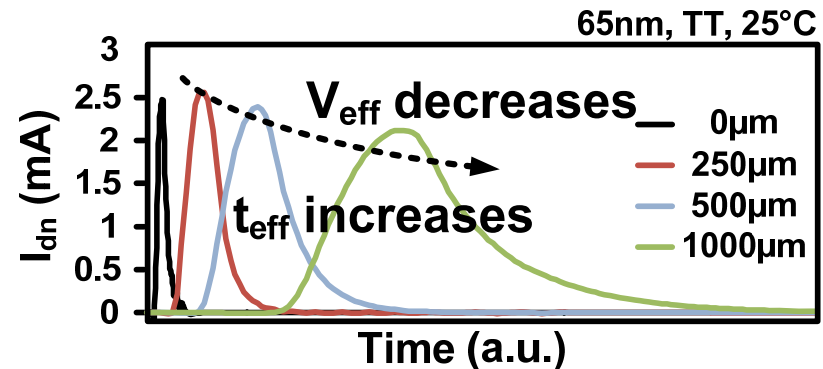
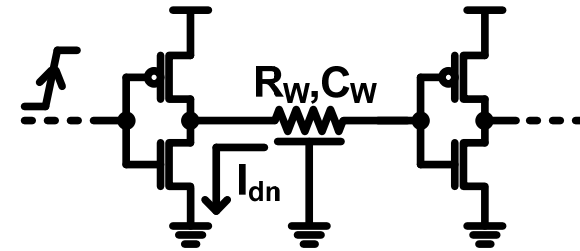
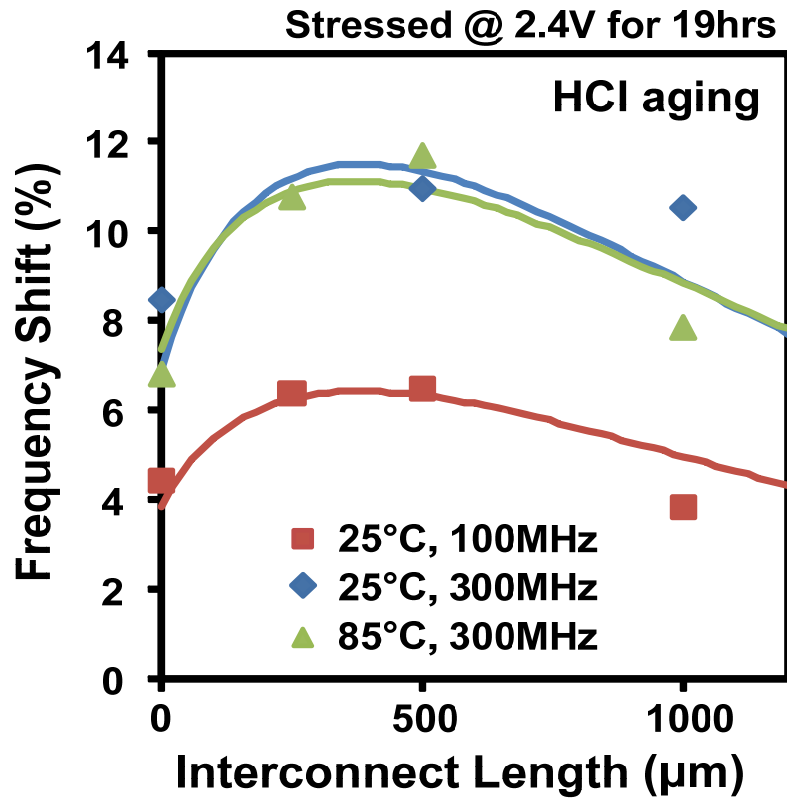
- BTI aging decreases with interconnect length
- HCI degradation peaks at $L=500\mu\text{m}$

BTI Aging vs. Interconnect Length



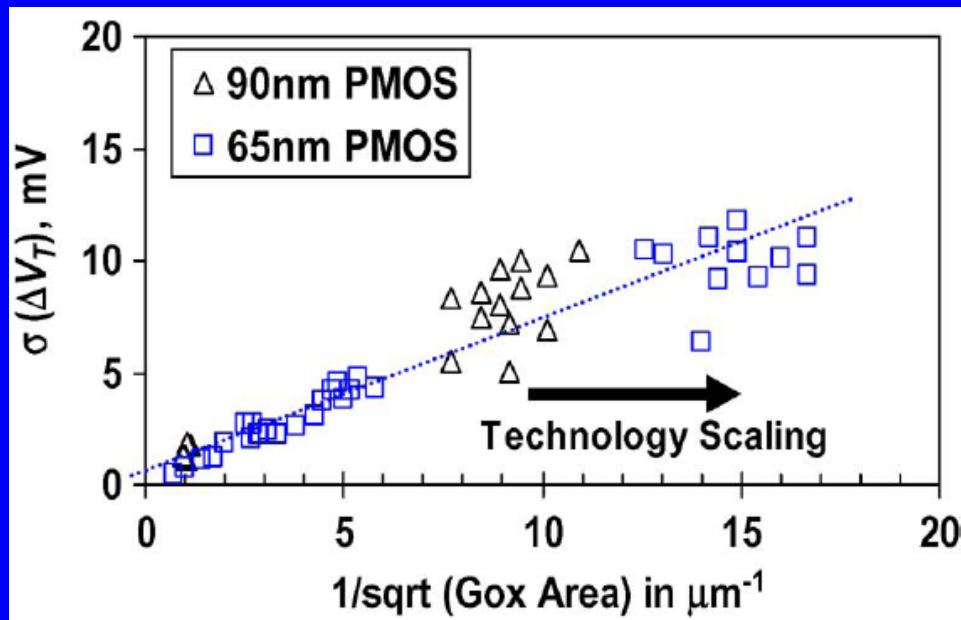
- BTI induced frequency degradation decreases with longer interconnect
- Longer transition time \rightarrow shorter PMOS stress duration \rightarrow Less BTI aging

HCl Aging vs. Interconnect Length



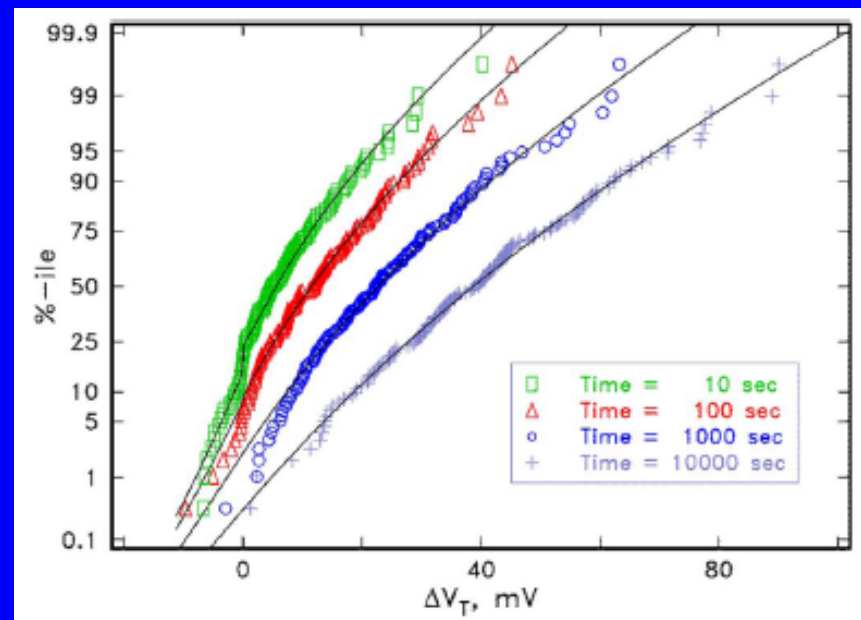
- HCl aging exhibits a non-monotonic behavior with respect to interconnect length
 - Current pulse width increases
 - Current peak decreases

Statistical Behavior of Aging



Spread in ΔV_t increases with scaling

S. Pae, et al., TDMR'08



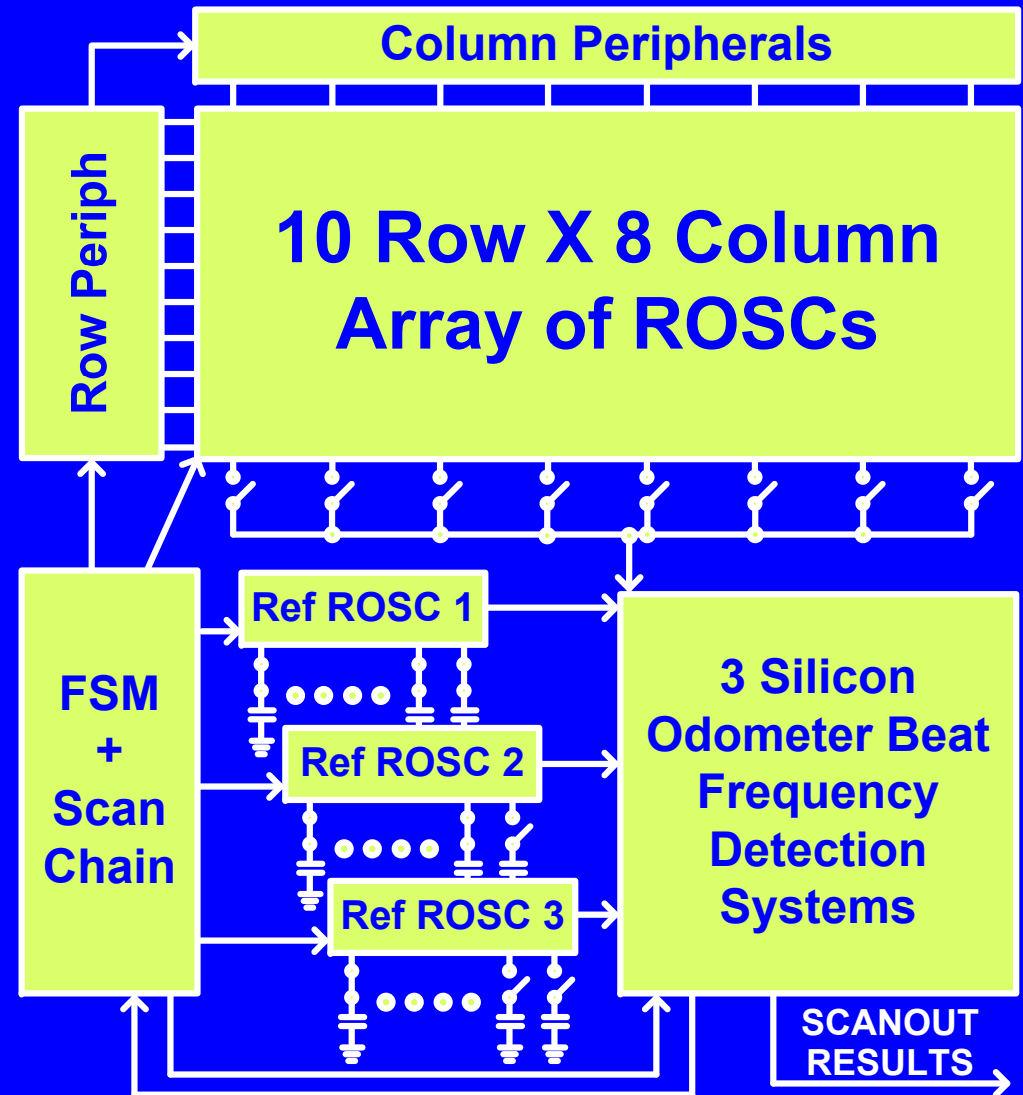
CDF of ΔV_t at different stress times

S. Rauch, TDMR, Dec. '07

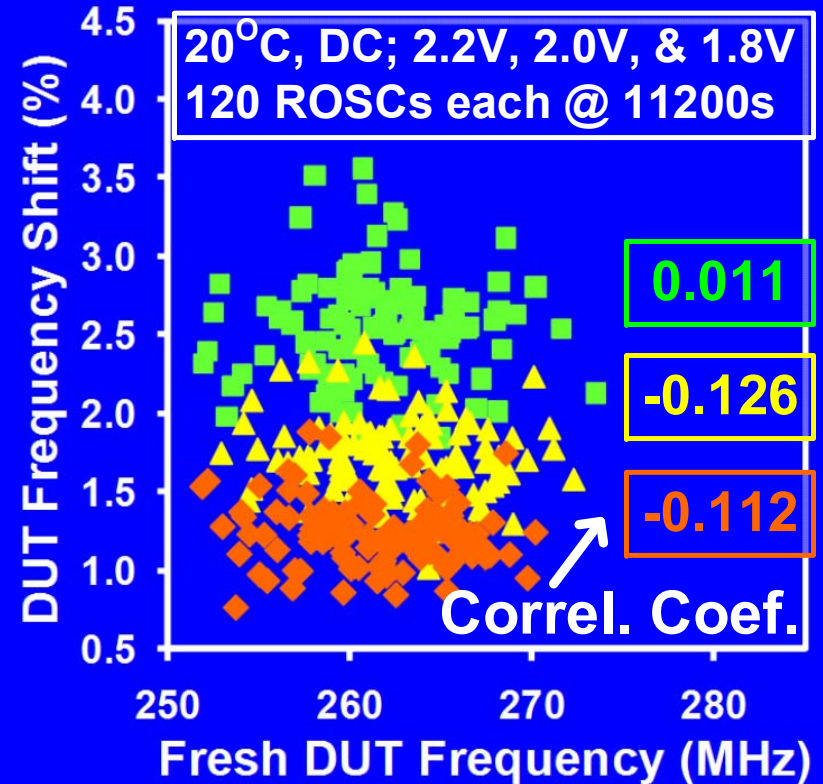
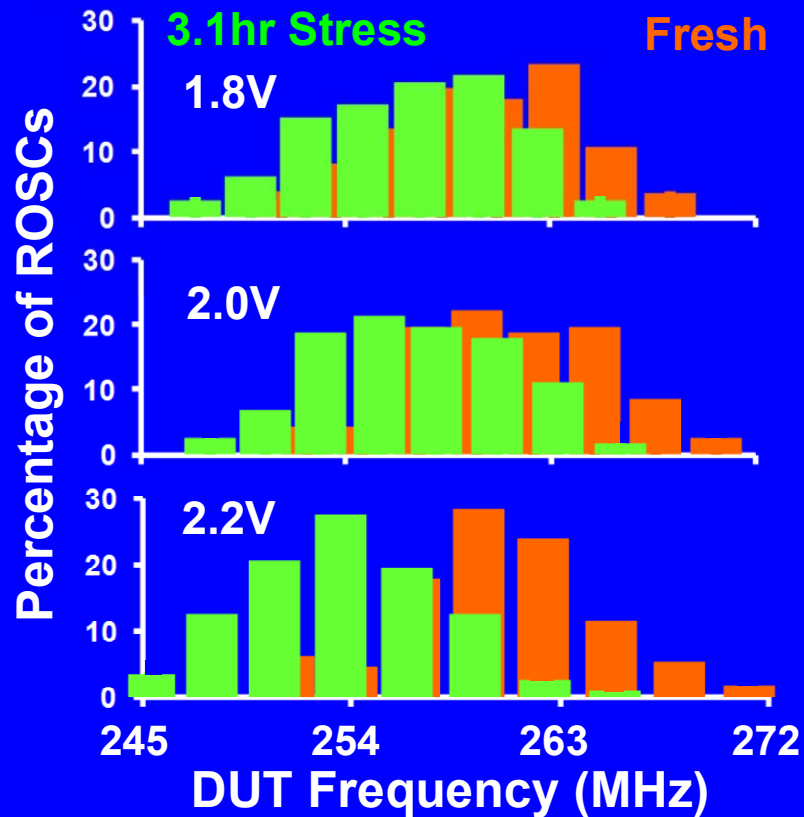
- Finite number and random spatial distribution of discrete charges \rightarrow NBTI & HCI variation
- Inversely proportional to $A_{\text{GATE}} \rightarrow$ worse with scaling
- Small number of aging measurements not sufficient to characterize aging

Statistical Reliability Monitor

- Need stressed & reference ROSC frequencies to be close
- Difficult, costly to tune each stressed ROSC
- Use multiple ref. ROSCs with different frequencies
- Cover the frequency distribution of the stressed array

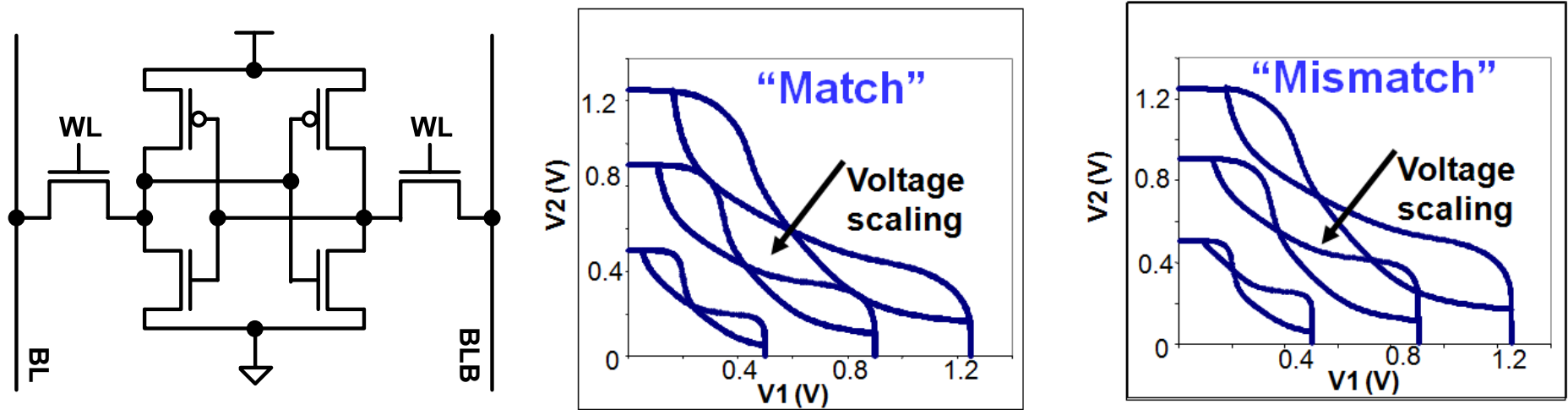


65nm Test Chip Data



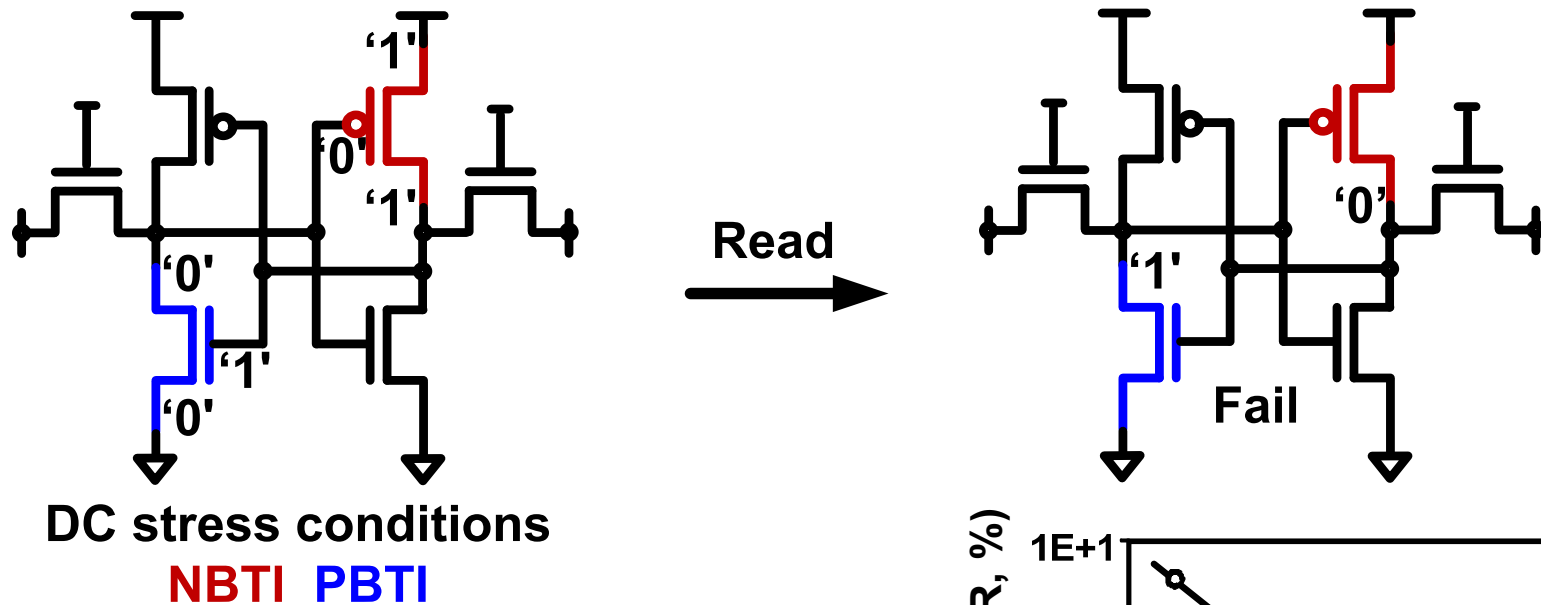
- Fresh and post-stress ROSC frequency PDFs
- No significant correlation of the frequency shift with fresh frequency

SRAM Memory Design Challenges at Low Supply Voltages

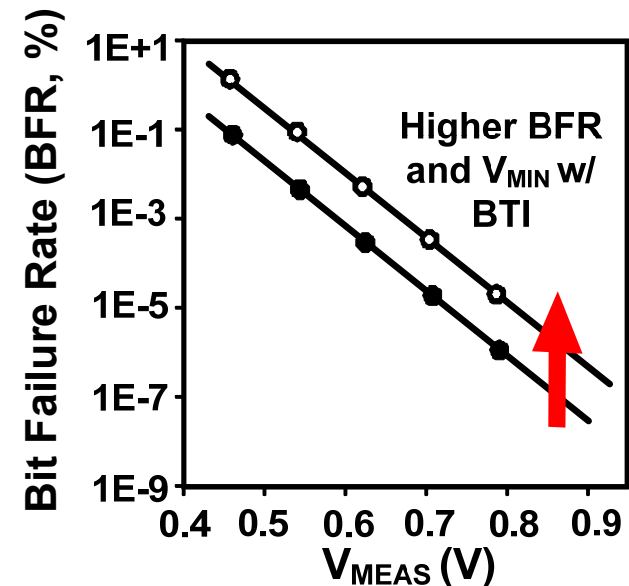


- **Ratio-ed operation leads to poor noise margin at low voltages for 6T SRAM cells**
- **Conflicting requirements: a stronger access transistor improves write margin but worsens read margin**

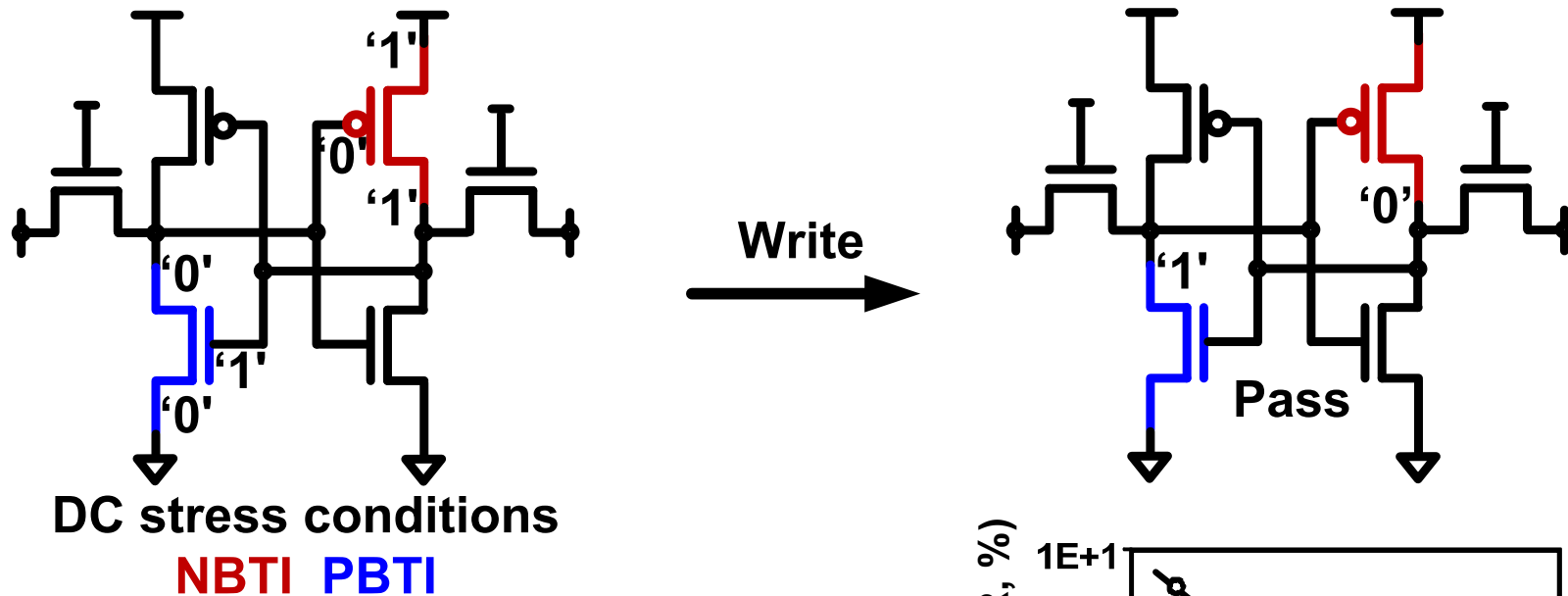
Impact of BTI on SRAM Read



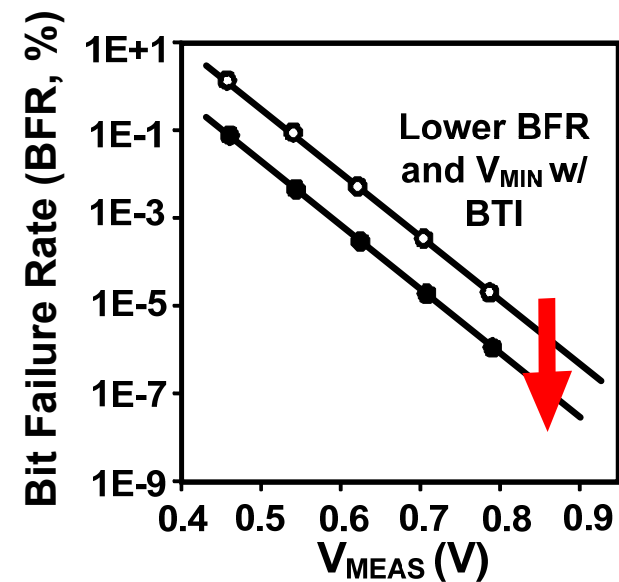
- With BTI: Read stability degrades
- Cell recovers on a fail



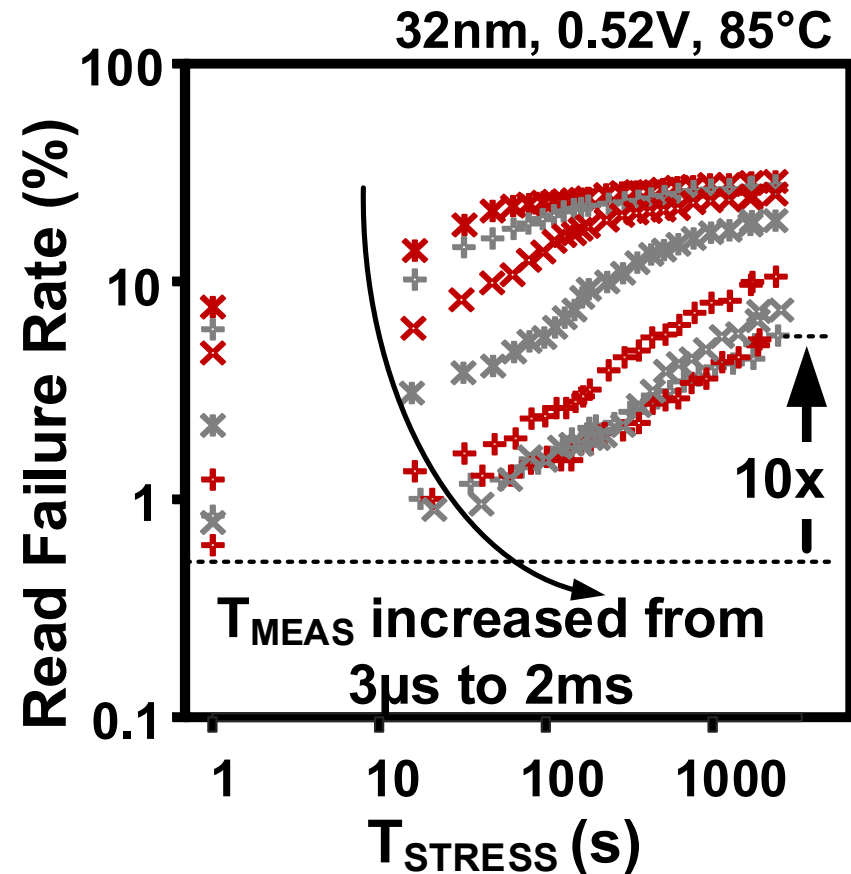
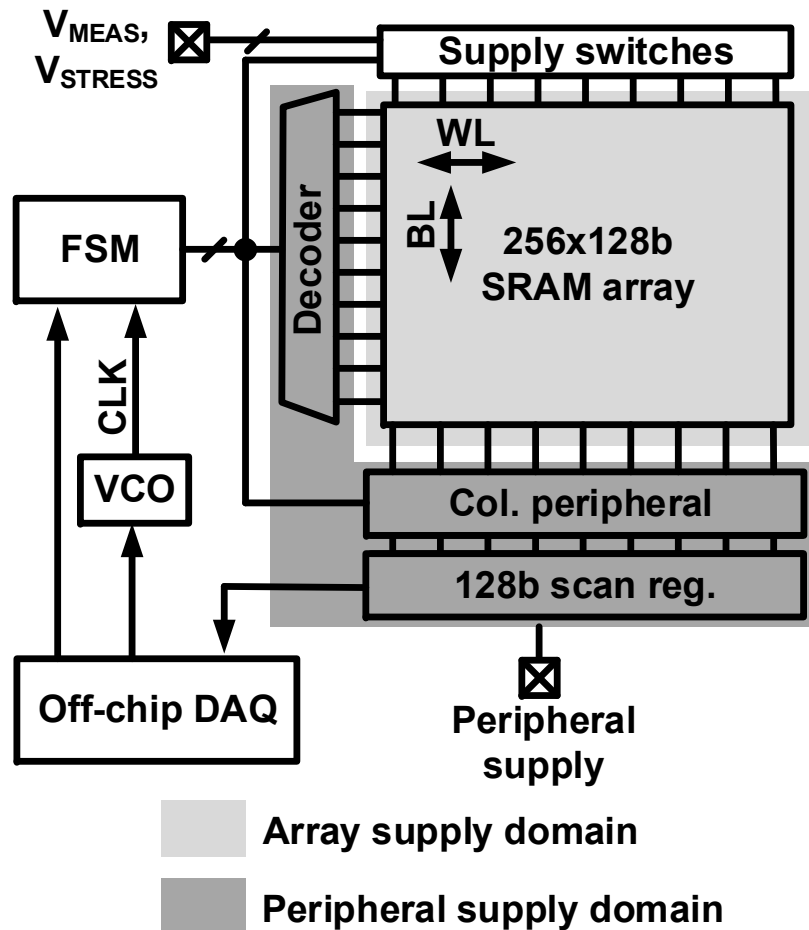
Impact of BTI on SRAM Write



- With BTI: Write stability improves or remains unchanged
- Cell recovers on a pass



Representative SRAM Reliability Macro

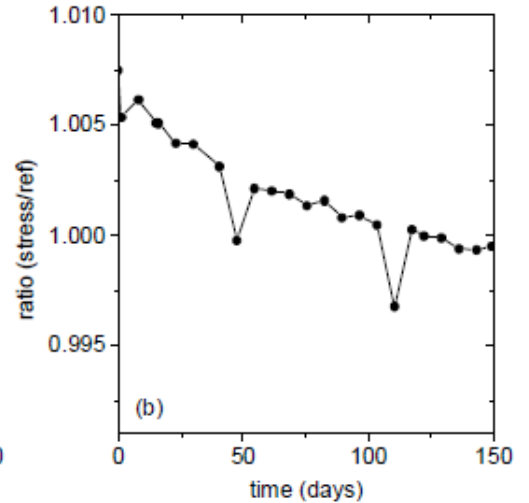
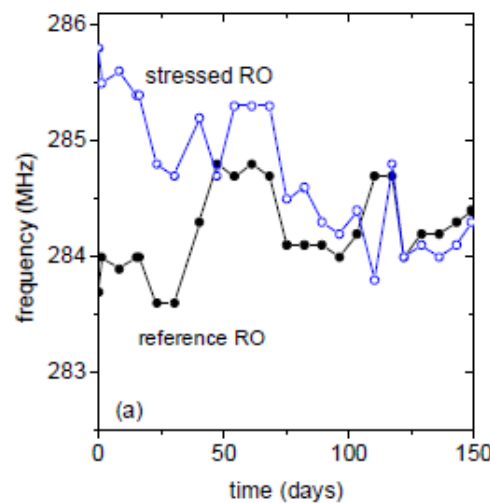
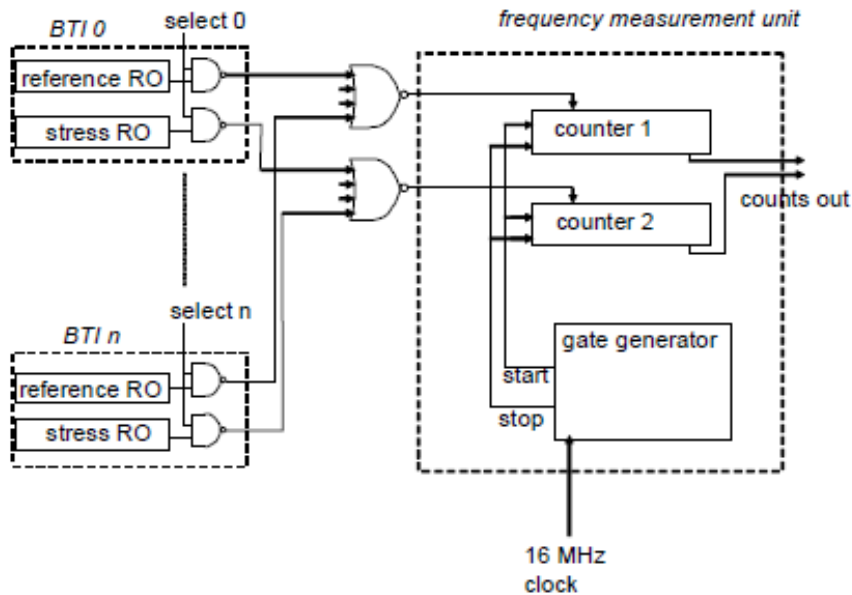


P. Jain, *et al.*, IEDM, 2012

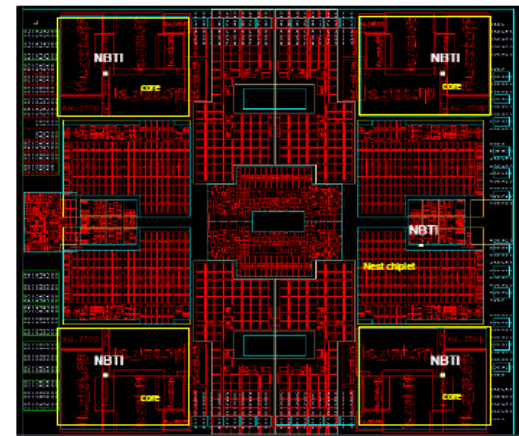
- Represents a product SRAM sub-array
- BIST function done by on-chip FSM with supply switches

Aging Monitor in IBM Microprocessors

Pongfei Flu, Keith Jenkins, IBM, IRPS 2013

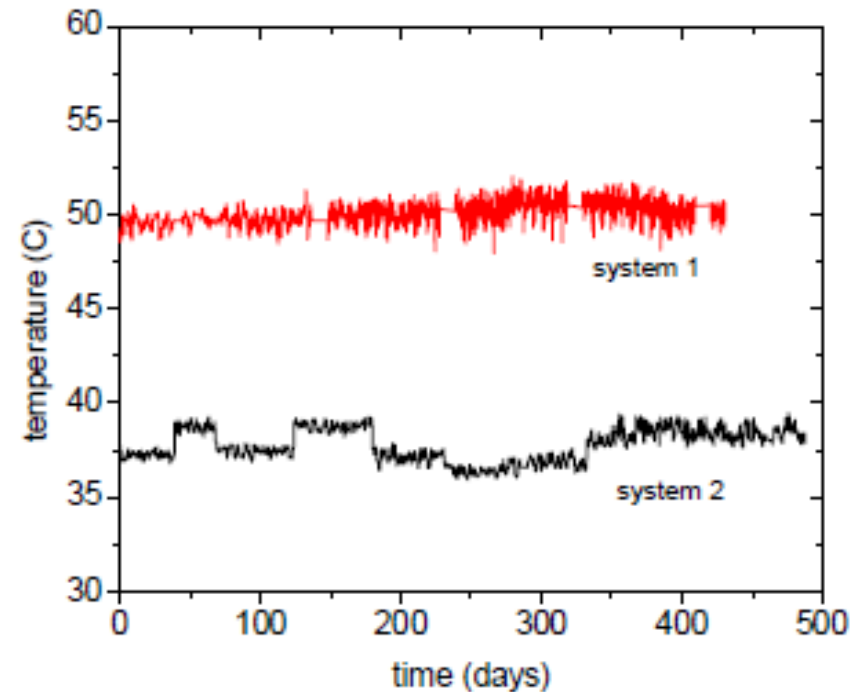
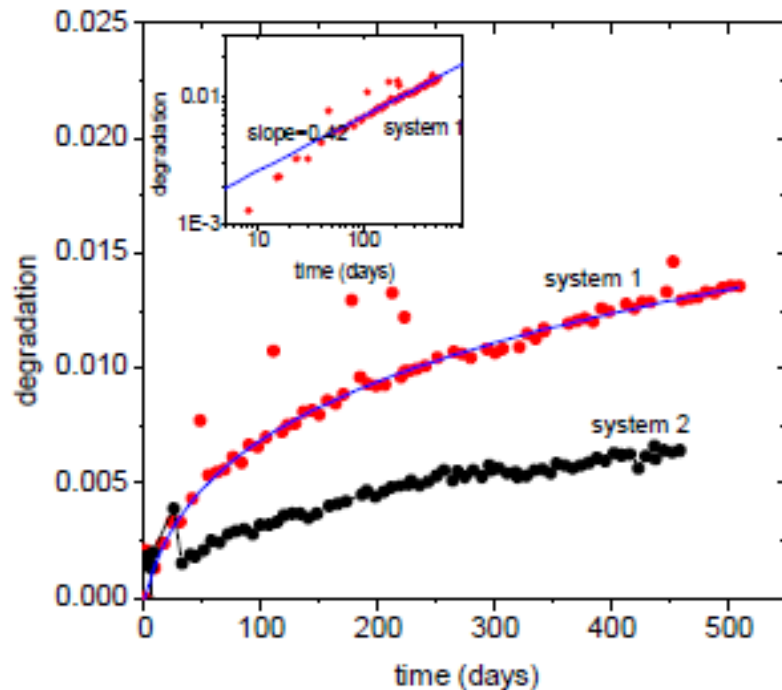


- Implemented on IBM's z196 Enterprise systems for long term degradation under real-use conditions.
- Over 500 days worth of ring oscillator degradation data from customer systems
- Other companies have aging monitors too, but they tend not to publish their work



Aging Monitor in IBM Microprocessors

Pongfei Flu, Keith Jenkins, IBM, IRPS 2013



- Time-zero problem: Some time will elapse between applying voltage (burn-in, test, operation) and making the first measurement → time-zero frequency is completely unknown → incorrect time slope of 0.42
- Use fitting parameters assuming $\Delta f = A(t-t_0)^n - At^n$ → time slope of 0.172

Aging Monitor in IBM Microprocessors

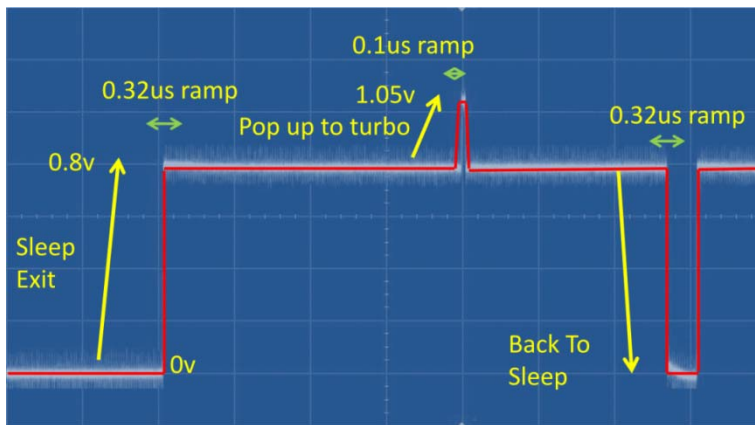
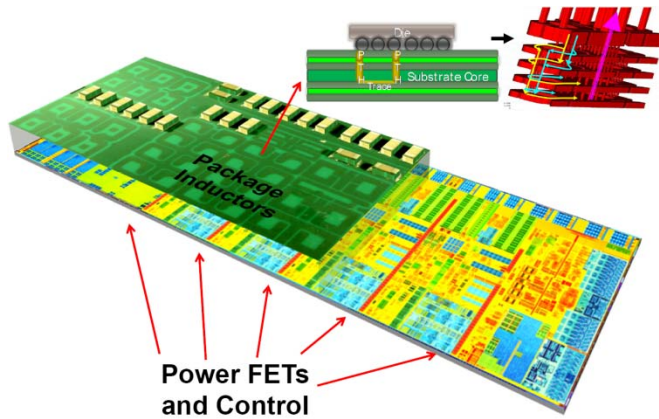
Pongfei Flu, Keith Jenkins, IBM, IRPS 2013

<i>Design Considerations</i>	<i>Examples of Practical Issues</i>	<i>Aging Sensor Implementation in IBM z196 Server [3]</i>
Type of Sensor	BTI, HCI, TDDDB, RTN, transient errors, memory bit failures, etc.	Ring Oscillator based BTI monitor for long-term frequency degradation measurement
Temporal Granularity	Sensing period, threshold setting, dynamic range, etc.	Sampling period: once a week
Spatial Granularity	Per CPU/GPU/memory, per functional unit, per sub-block, etc.	Total: 5 sensors per chip; One sensor per core (x4 cores) plus one sensor in L2 cache
Stress and Measurement Condition	AC vs. DC, accelerated vs. usage condition, fast measurement	AC stress, usage condition, 0.5ms measurement time
Communication	Between data gathering sensor, across sensors, between sensors and processor	Sensors are integrated with IBM z196 pervasive infrastructure with firmware support
Interface and Protocol	Interrupt based, polling, event alarms, performance counter based, etc.	Interrupt based in-field frequency degradation measurement
Testing and Calibration	Similar to any other on-chip monitor circuit	Time 0 frequency shift unknown since first sample is taken after some stress

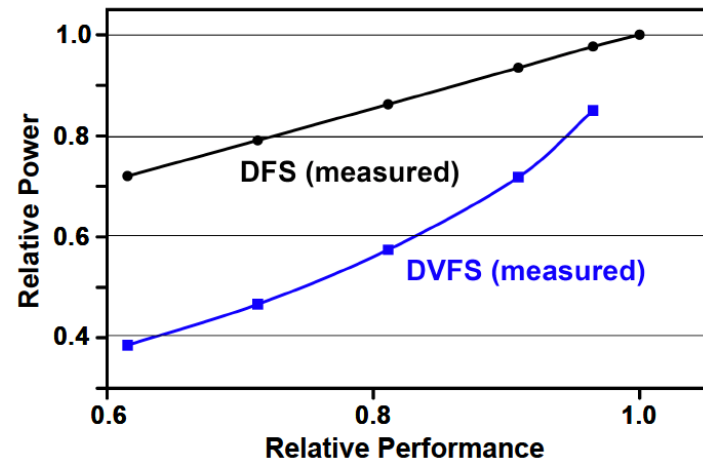
Outline

- Device Reliability Issues
- Monitors and Measurements
- **Effects in NTV Processors**
- Summary

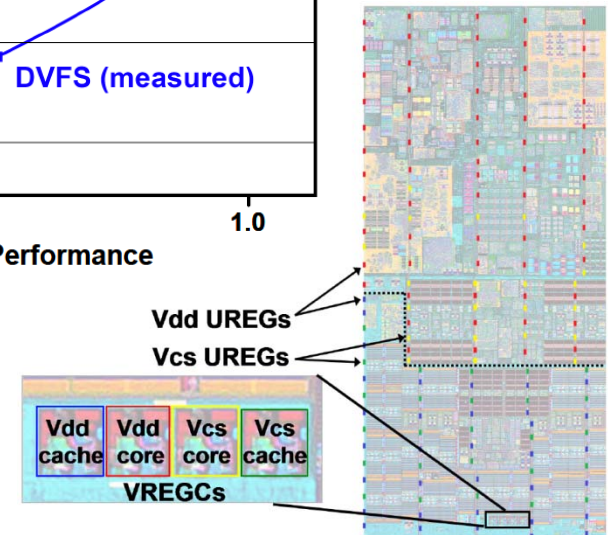
DVFS Systems in ISSCC 2014



22nm Intel Haswell processor
N. Kurd, *et al.*, ISSCC, 2014



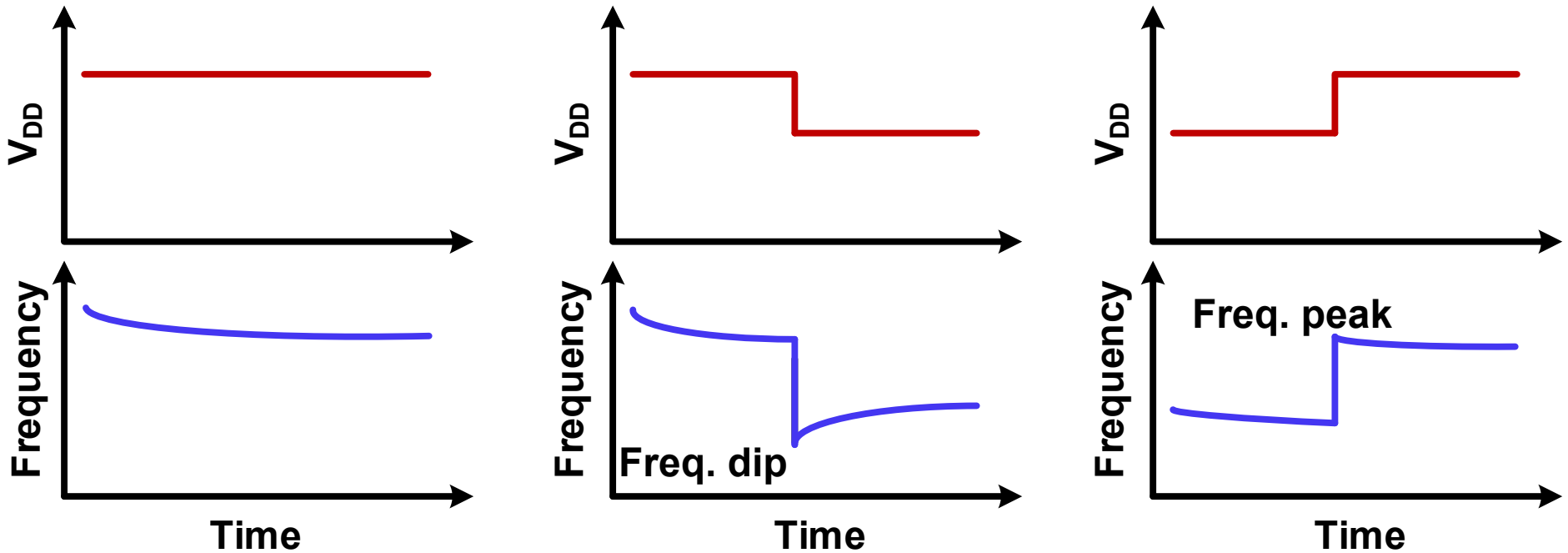
<1% area overhead



22nm IBM POWER8 processor
Z. Toprak-Deniz, *et al.*, ISSCC, 2014

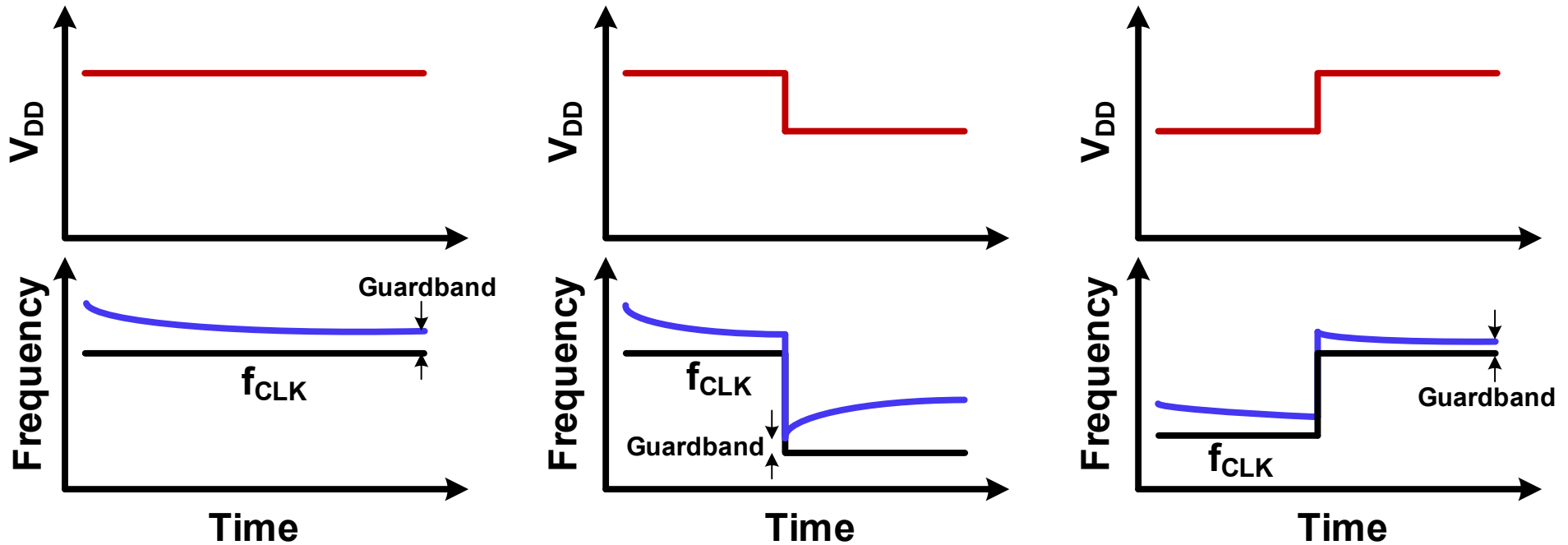
- Latest trends: On-chip distributed VRM (fast transients, supply noise suppression), per-core DVS, NTV/Turbo

Frequency Fluctuation in DVFS (BTI Example)



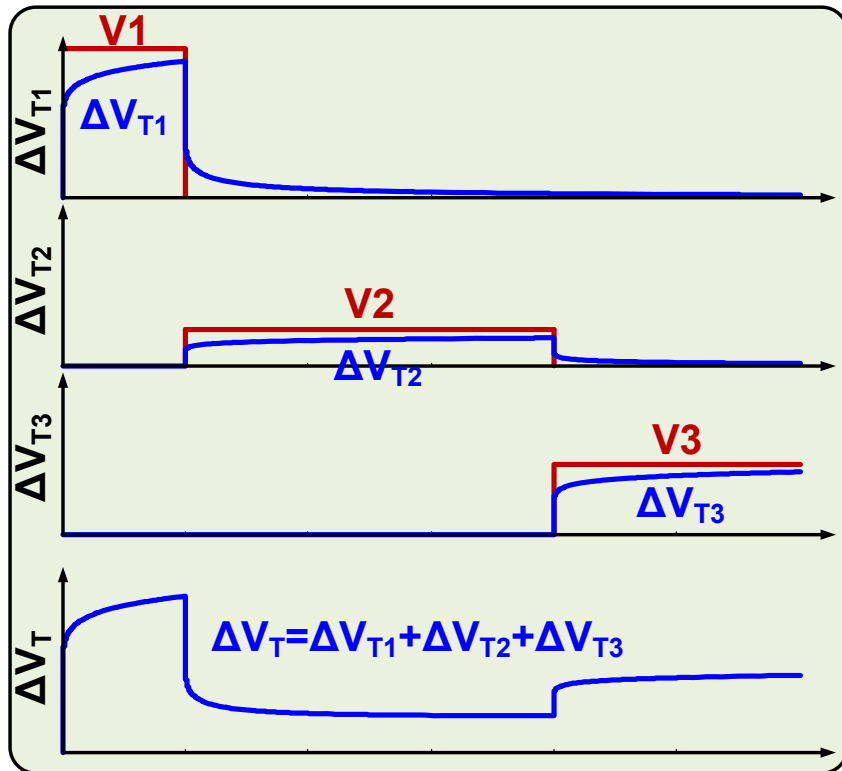
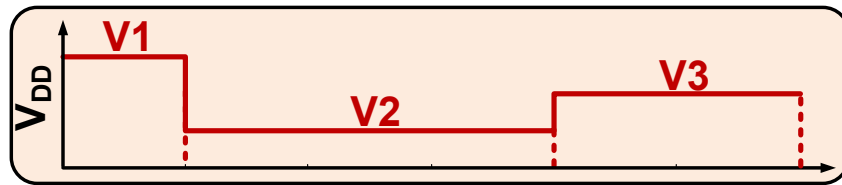
- **Constant V_{DD} : Frequency degrades with stress**
- **High V_{DD} to low V_{DD} : Freq. dips due to lower V_{DD} followed by recovery**
- **Low V_{DD} to high V_{DD} : Freq. jumps and then degrades**

Frequency Fluctuation in DVFS (BTI Example)

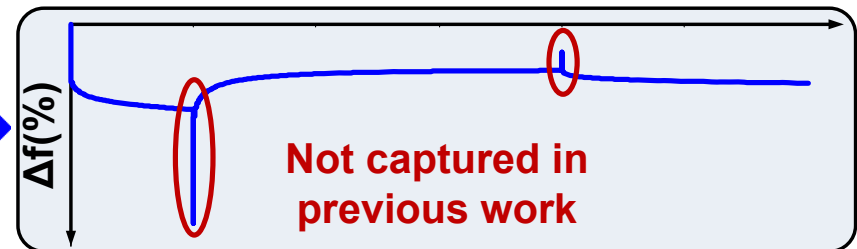


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Modeling Approach using Superposition



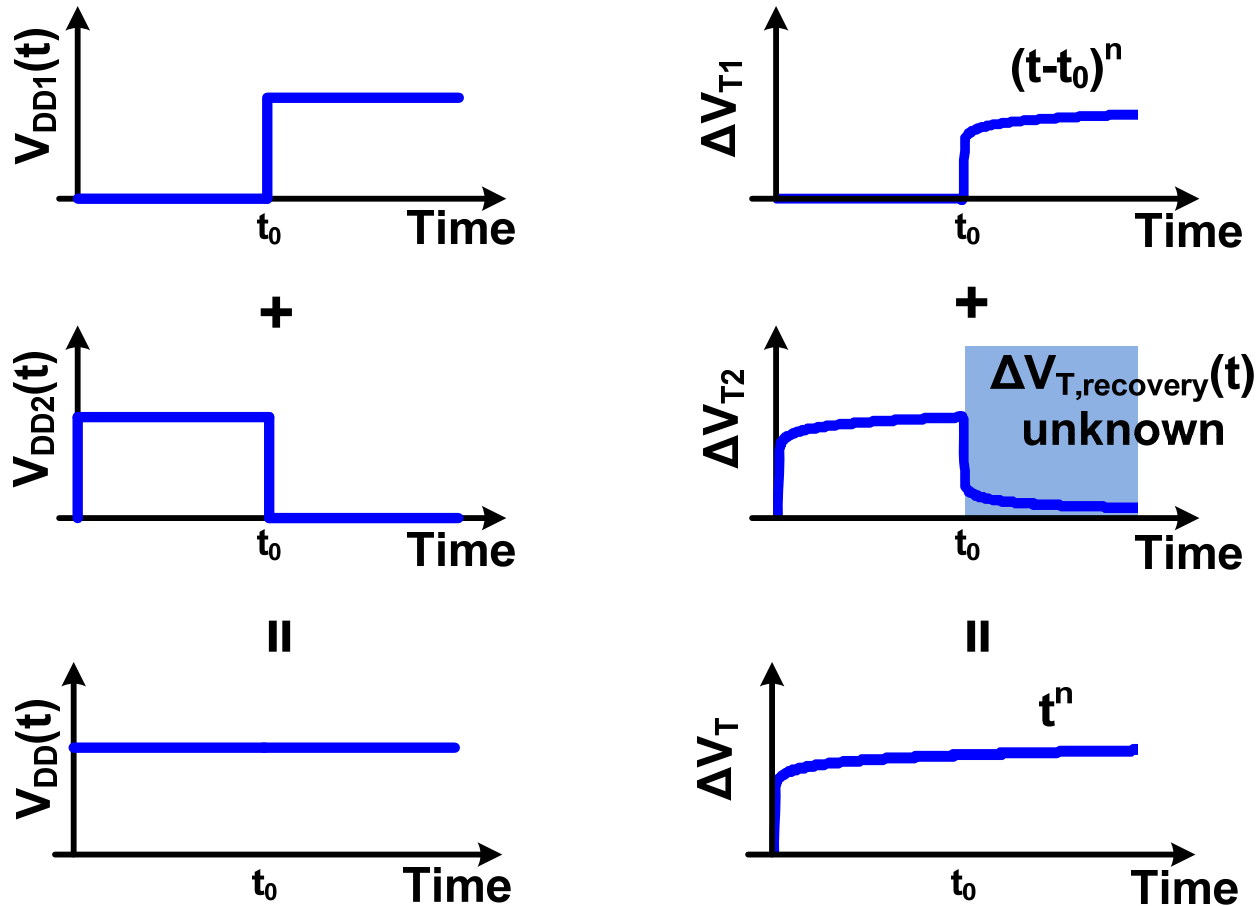
Time (a.u.)



Time (a.u.)

- Rationale for empirical superposition method
 - Complicated V_{DD} trace can be broken down into multiple pulses
 - Suitable for long-and short-term, DC and AC
 - Computation is more efficient, short runtime

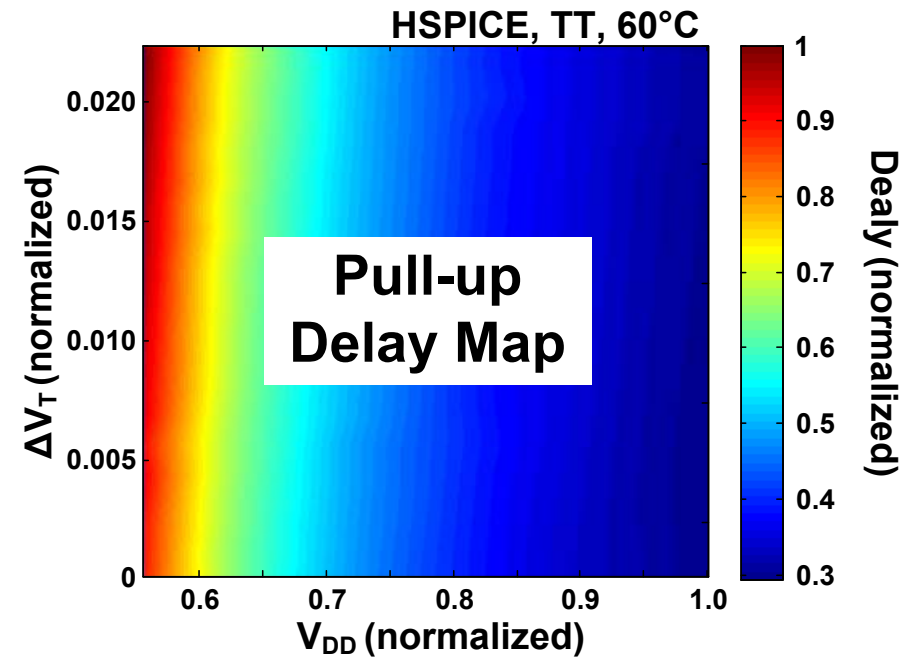
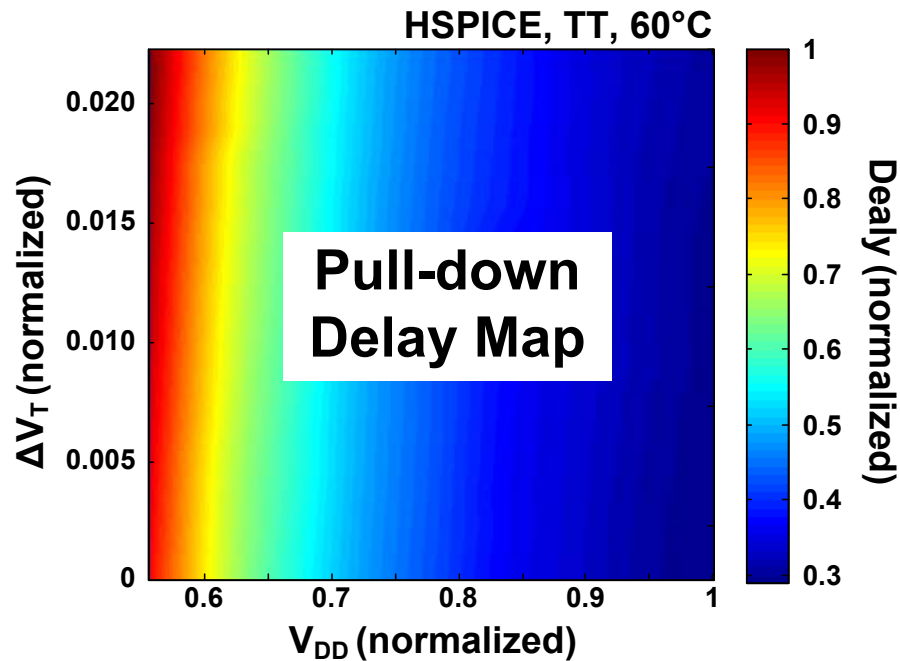
BTI Recovery Model using Superposition



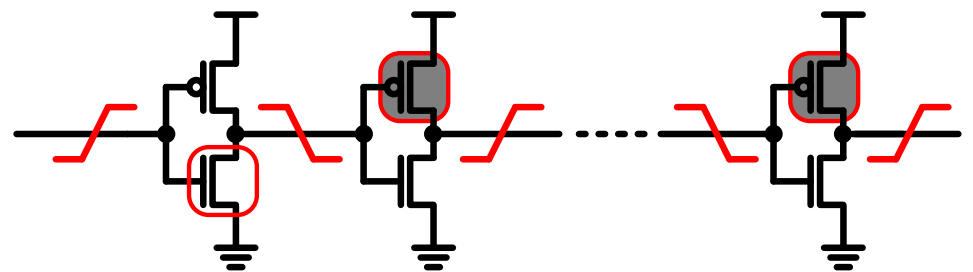
- Stress model: t^n (power law)
- Recovery model derived from superposition property:

$$\Delta V_{T, \text{recovery}}(t) = t^n - (t-t_0)^n$$

Translating V_T Shift to Delay Shift

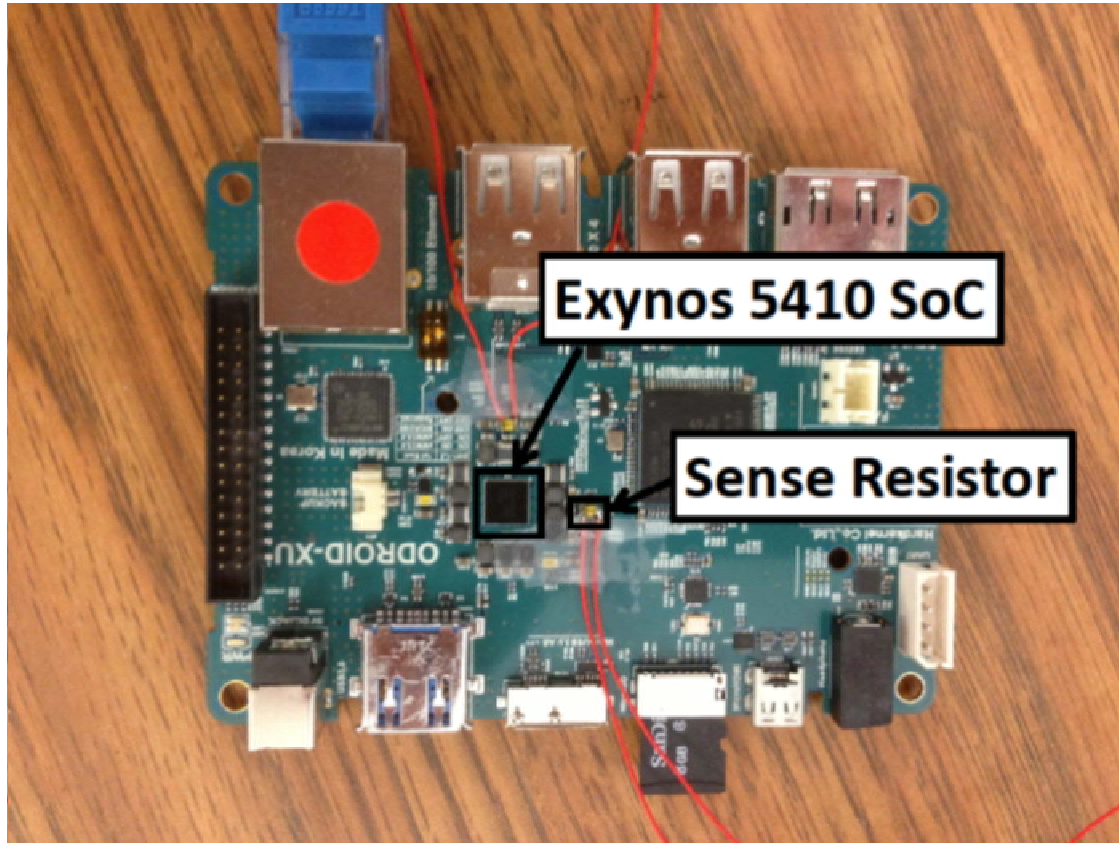


- ROISC mimics logic path
- Translate ΔV_T to pull-up, pull-down delay



 Pull-down Delay  Pull-up Delay

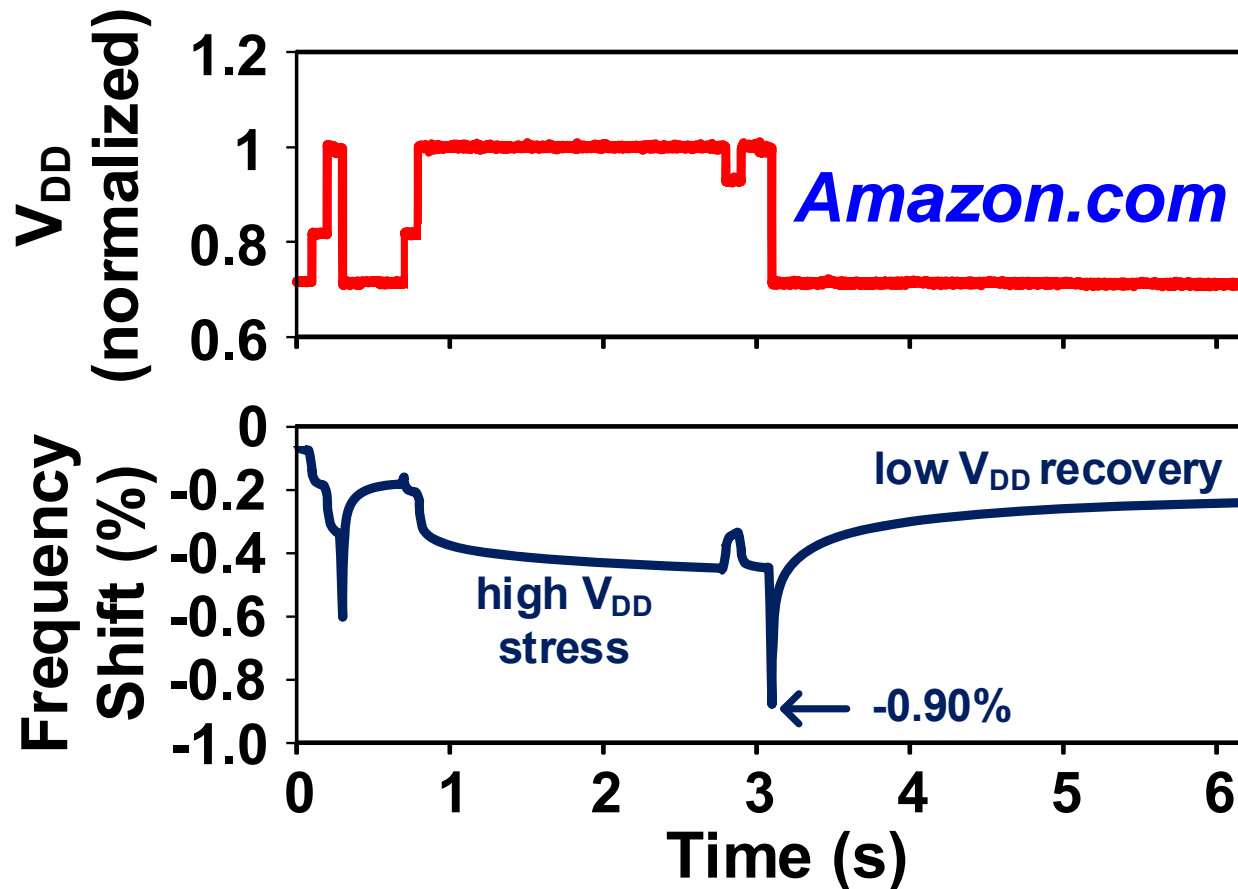
Android Development Board for Collecting DVFS Traces



Processor	ARM Cortex A15
System	Samsung Exynos 5410 SoC
Process	28nm
Frequency	0.8 – 1.8 GHz
Voltage	0.9 – 1.25 V
DVFS meas.	National Instr. DAQ
Sampling frequency	1000 samples per second
Linux kernel	v 3.4.5
Operating system	Android v 4.2.2

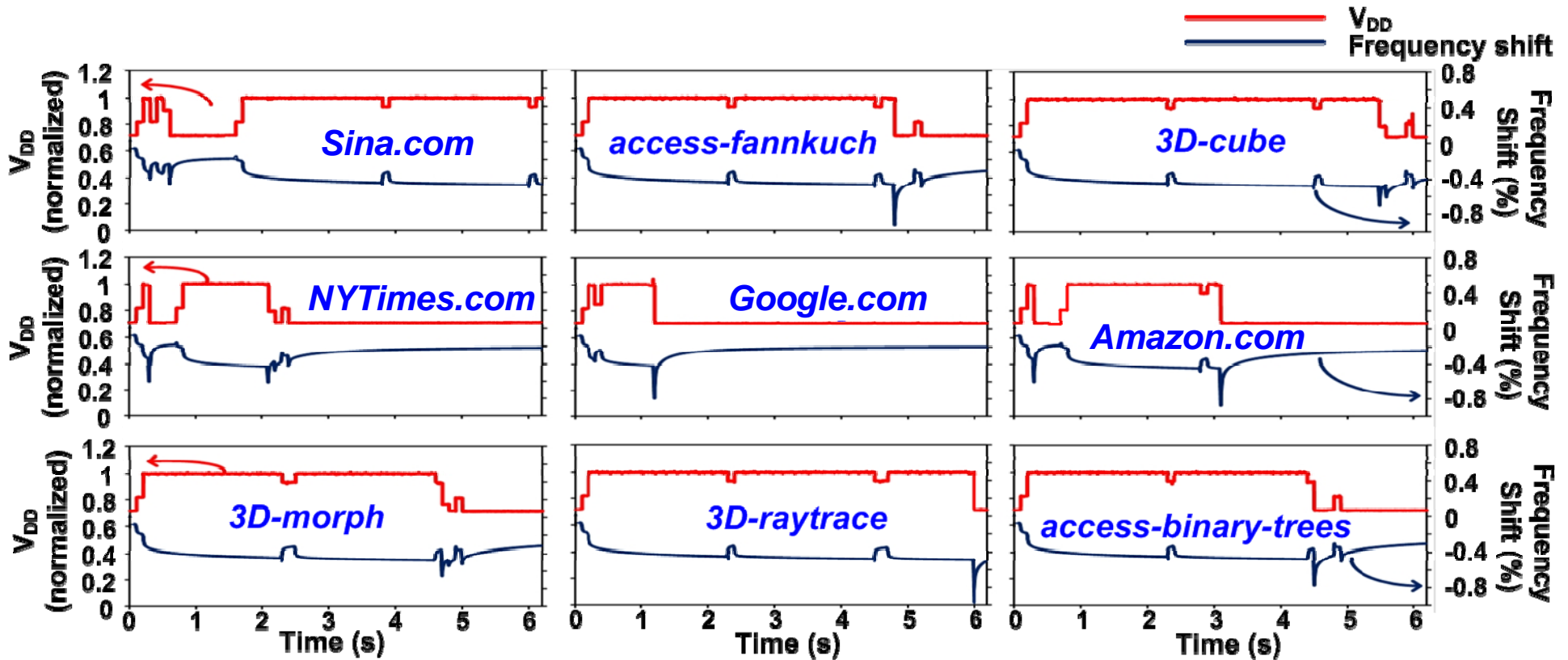
- V_{DD} and operating frequency collected in real time
- Navigating websites, running benchmark applications

Sample Waveform and Estimated Frequency Shift



- High V_{DD} duration: Freq. degrades with time
- Low V_{DD} duration: Freq. shift dips and then recovers

Applying Model to Other DVFS Traces



- **Worst case frequency dip**
 - 3D-raytrace: $\Delta f=1.0\%$ at $t=6s$ when V_{DD} drops by 29% after staying in high V_{DD} mode for 5.8s

Summary

- Power wall (2000) → Variability wall (2010) → Reliability wall (2020)
 - Example: NTV + RDF + BTI
- Aging sensor deployed for the first time in a commercial processor (IBM z systems)
- Per-Core DVFS with sub-microsecond ramp time becoming a standard feature in new processors
- Turbo boost + NTV: Best of both worlds in terms of power and performance, but presents new reliability challenges