Mitigating Parameter Variation with Dynamic Fine-Grain Body Biasing

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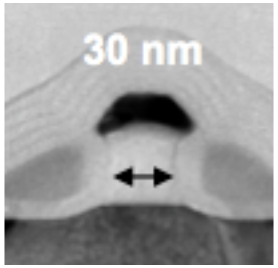
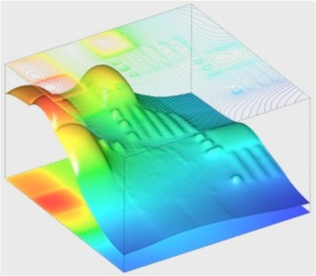
Parameter variation: roadblock to scaling

Process Variation



Temperature Variation



Supply Voltage Variation

Parameter variation: roadblock to scaling

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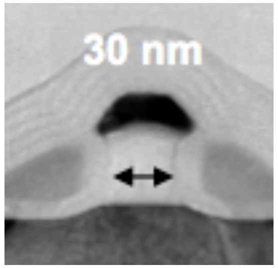

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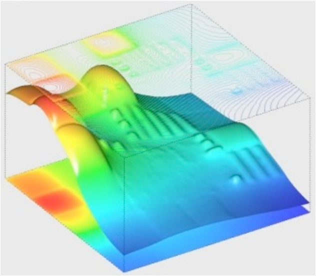
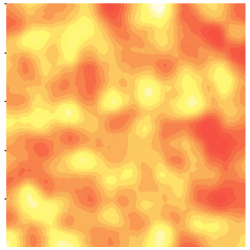
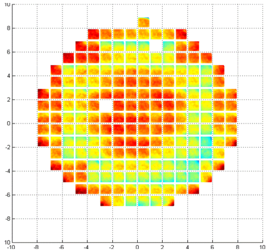


Within die (WID)



Die-to-die (D2D)



Parameter variation: roadblock to scaling

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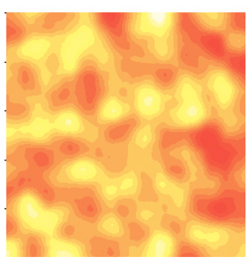
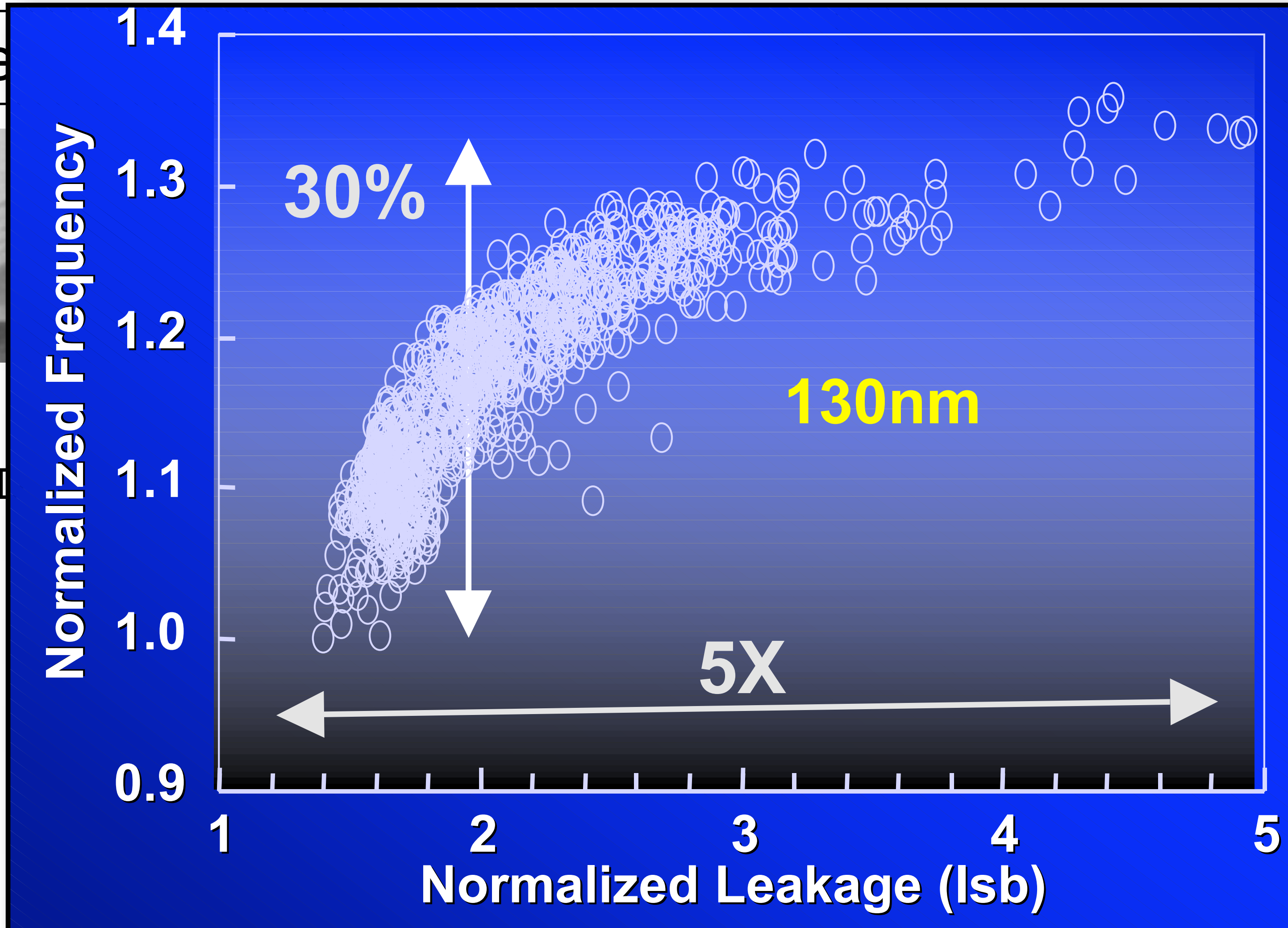
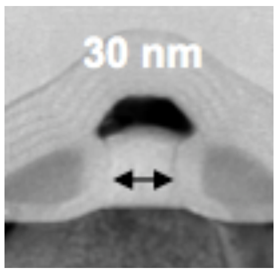




[Shekhar Borkar, Intel Corp.]

Technology scaling faces a major roadblock

Process Variation



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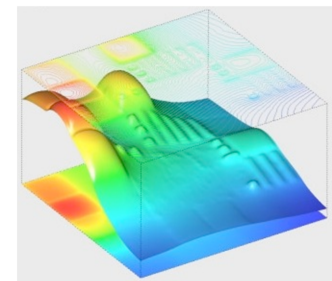


Threshold Voltage (V_{th})

Chip frequency

Chip leakage power

Body biasing

- Well known technique for V_{th} control
- A voltage is applied between source/drain and substrate of a transistor
  - Forward body bias (FBB) V_{th} ↓ Freq ↑ Leak ↑
  - Reverse body bias (RBB) V_{th} ↑ Freq ↓ Leak ↓
- Key knob to trade off frequency for leakage

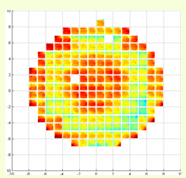
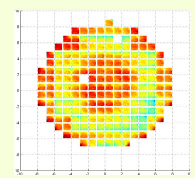
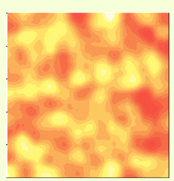
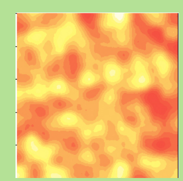
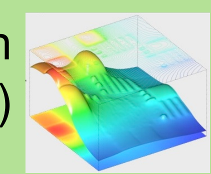
Frequency

Leakage power

Frequency

Dynamic power

Body bias design space

Time / Space	Static BB fixed for chip lifetime	Dynamic BB changes with T and workload
Chip-wide	 D2D V_{th} Variation [Intel Xscale] [Intel's 80-core chip]	 D2D V_{th} Variation T Variation
Fine-grain	 WID V_{th} Variation [Tschanz et al]	 WID V_{th} Variation T Variation (space and time) 

Body bias design space

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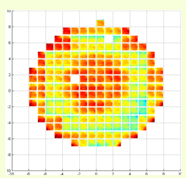
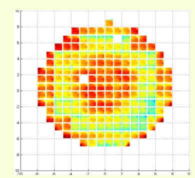
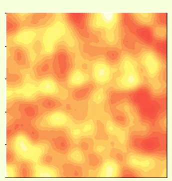
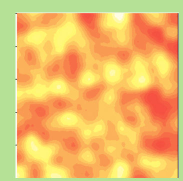
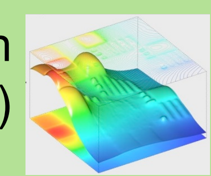
Chip-wide	 D2D V_{th} Variation [Intel Xscale] [Intel's 80-core chip]	 D2D V_{th} Variation T Variation
Fine-grain	 WID V_{th} Variation **S-FGBB** [Tschanz et al]	 WID V_{th} Variation **D-FGBB** (space and time) 

Outline

- Background on S-FGBB
- Dynamic fine-grain body biasing (D-FGBB)
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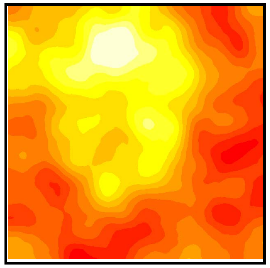
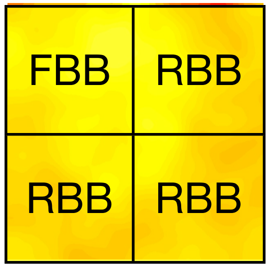
Static fine-grain body biasing

[Tschanz et al, ISSCC 2002]

V_{th} variation

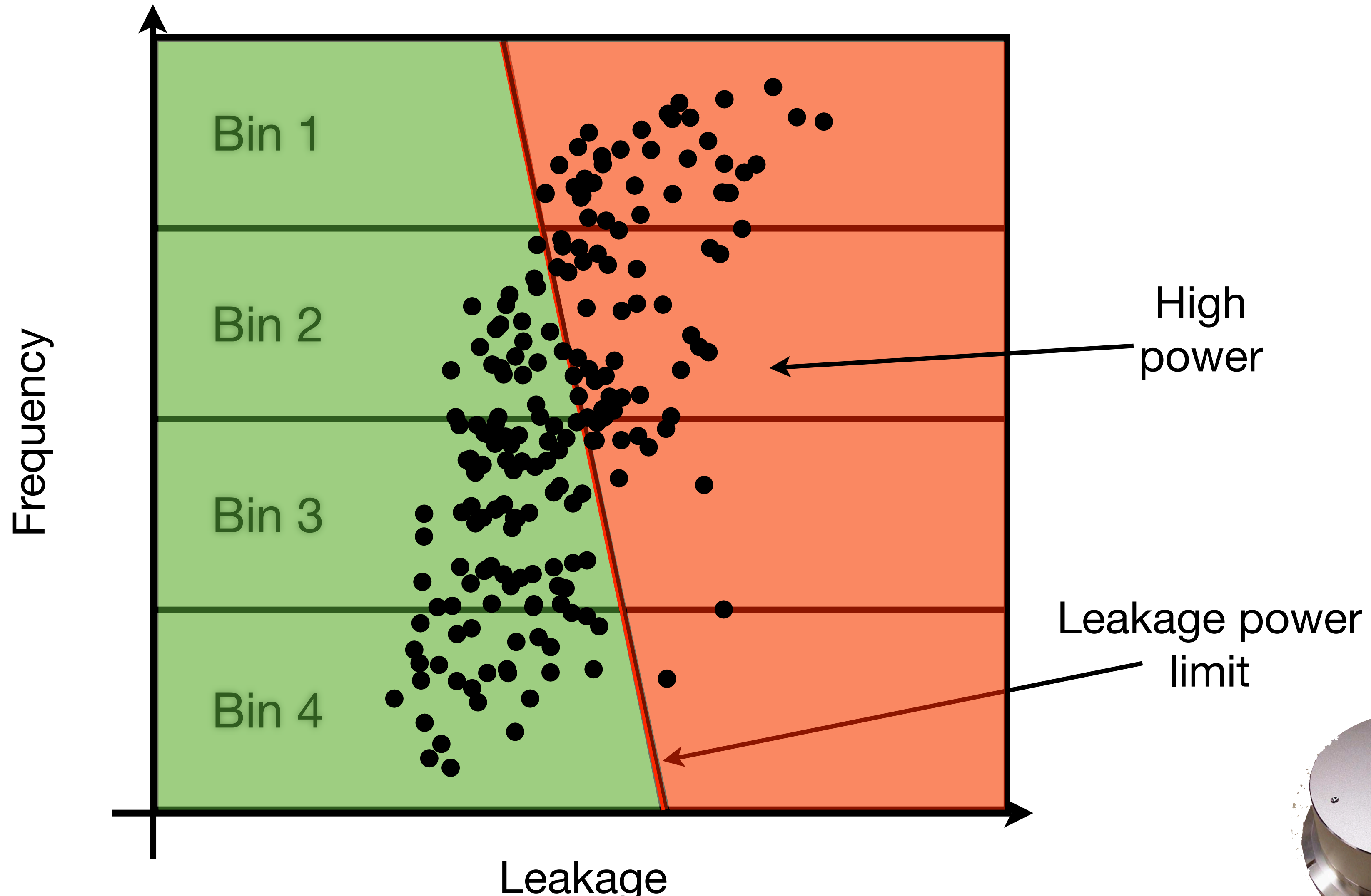


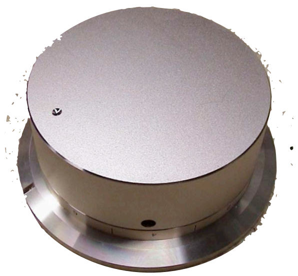
Fine Grain Body Bias



- The chip is divided in BB cells
  - Slow cells receive FBB - increase speed
  - Leaky cells receive RBB - save leakage
- The result is reduced WID variation (delay, power)
- BB voltages determined at manufacturing
- Fixed for the lifetime of the chip

Frequency binning





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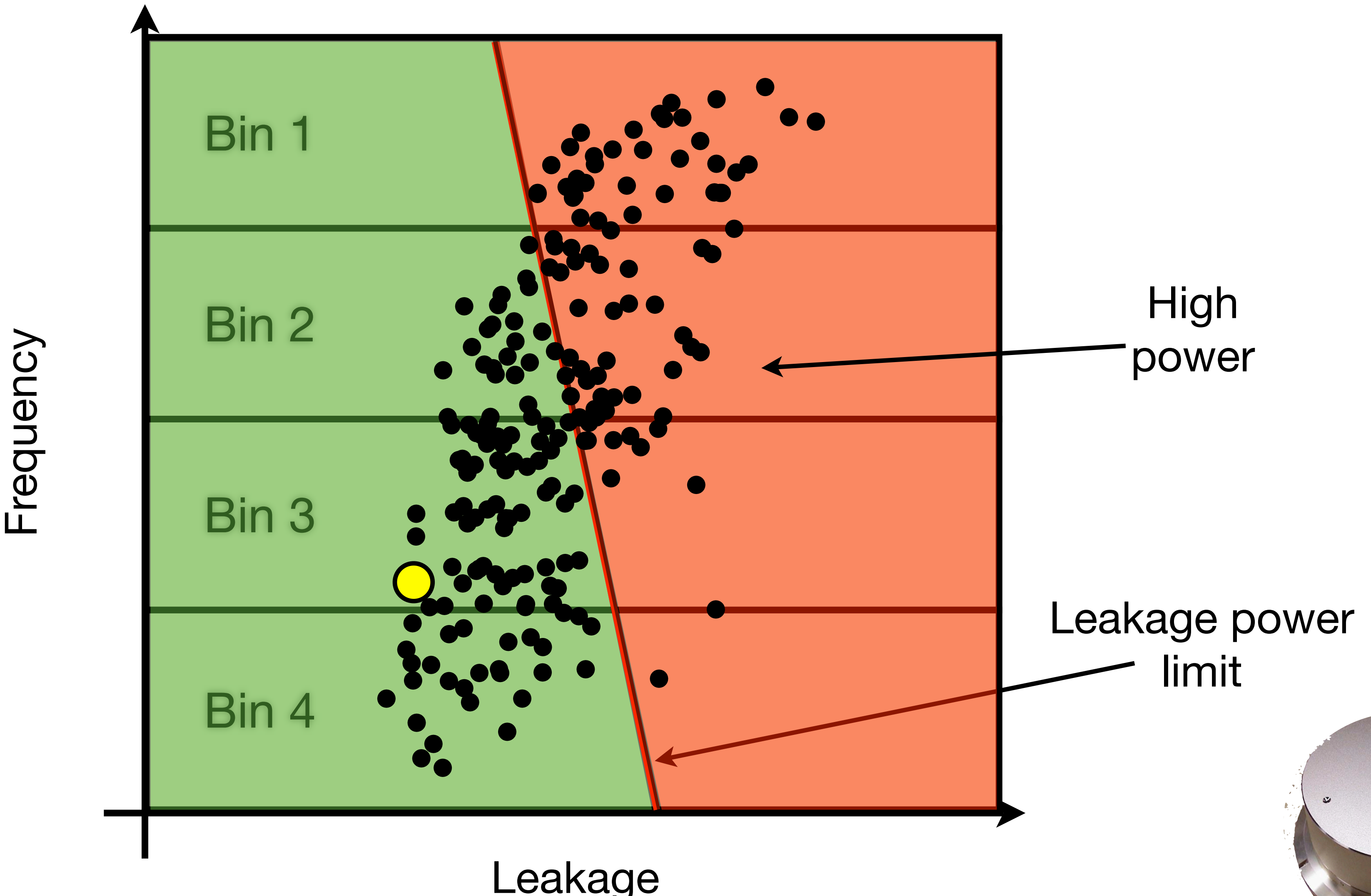

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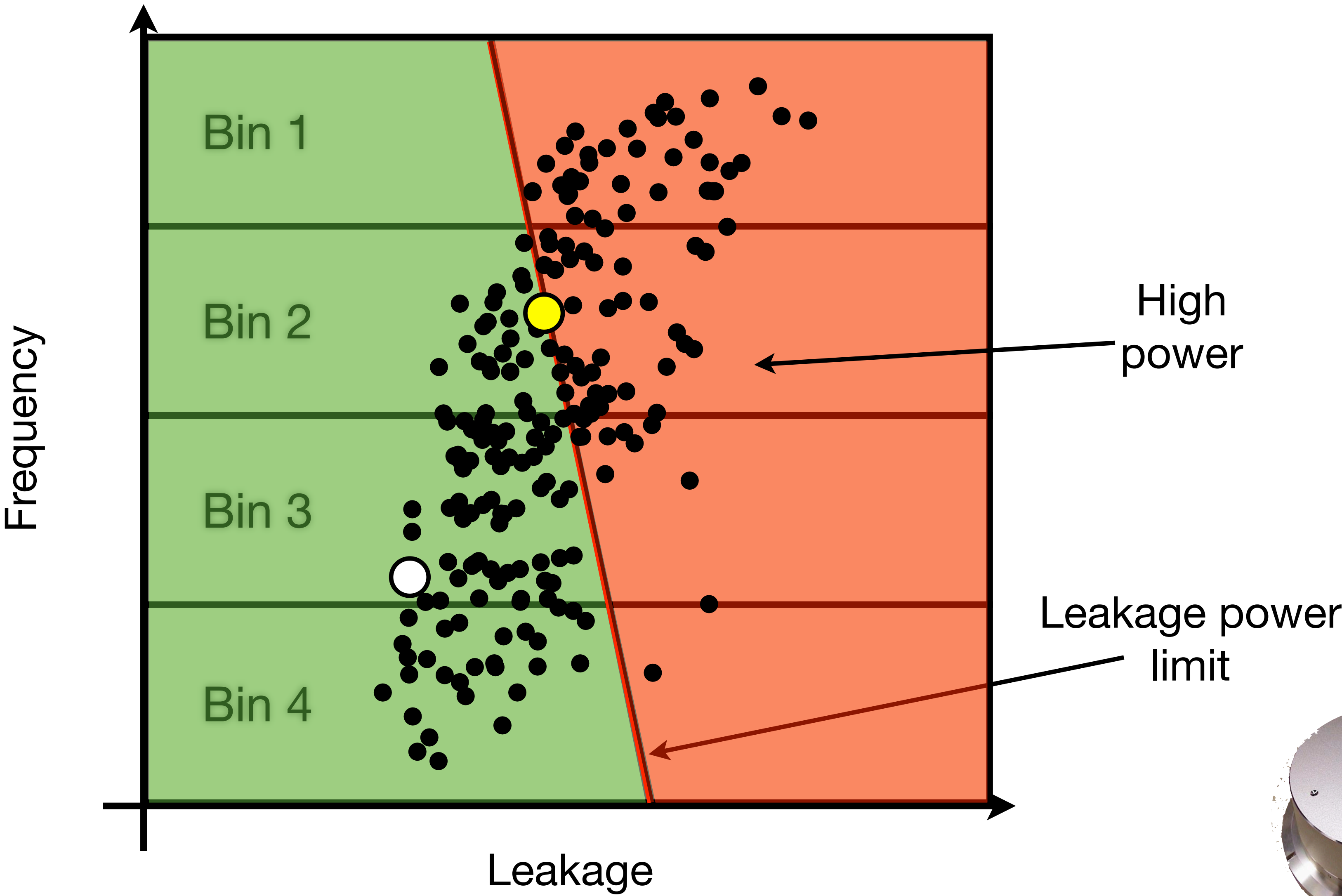

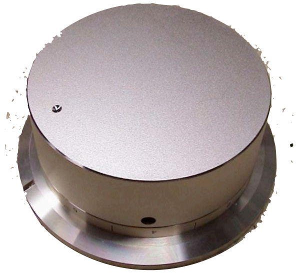

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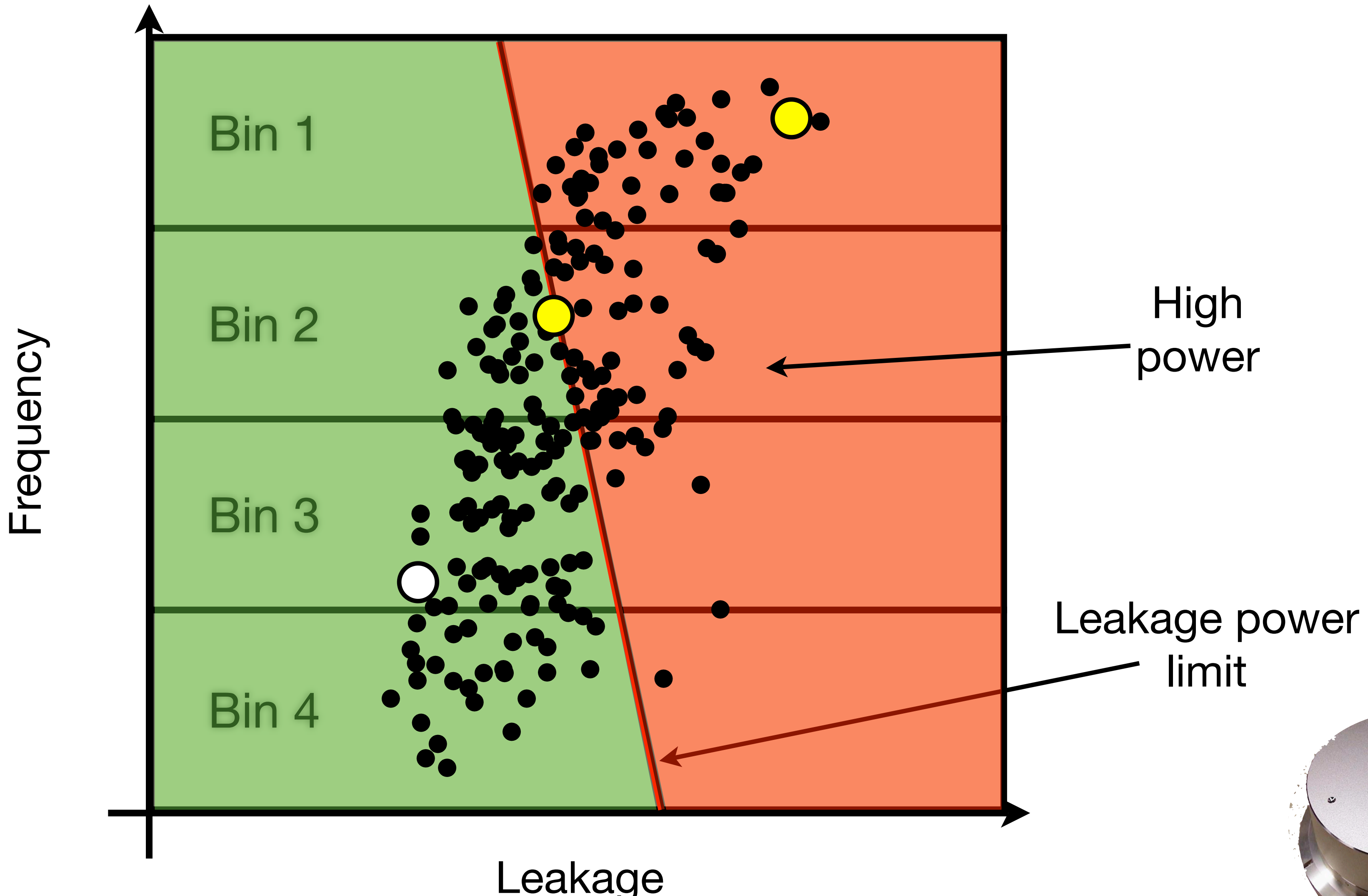
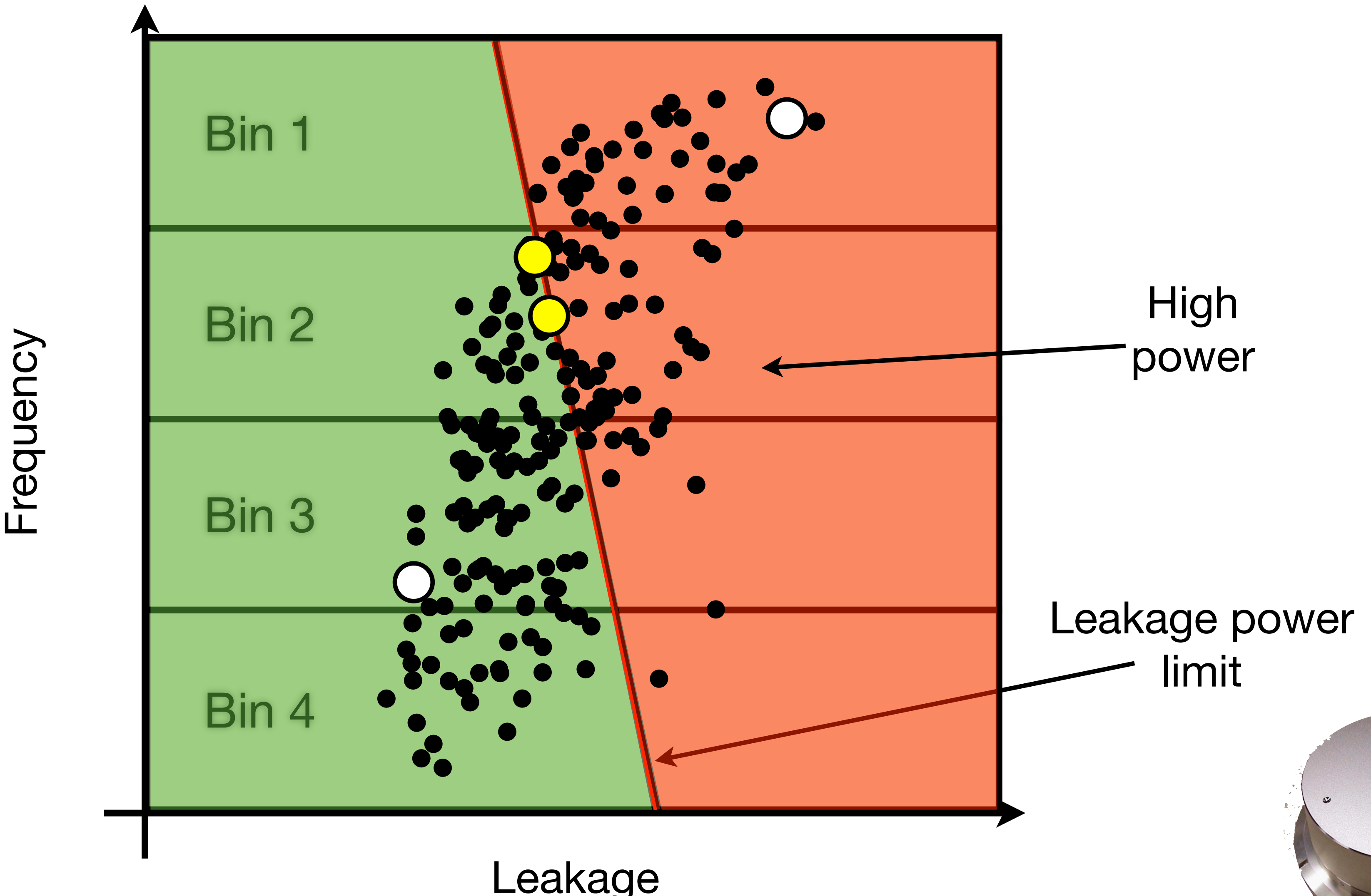
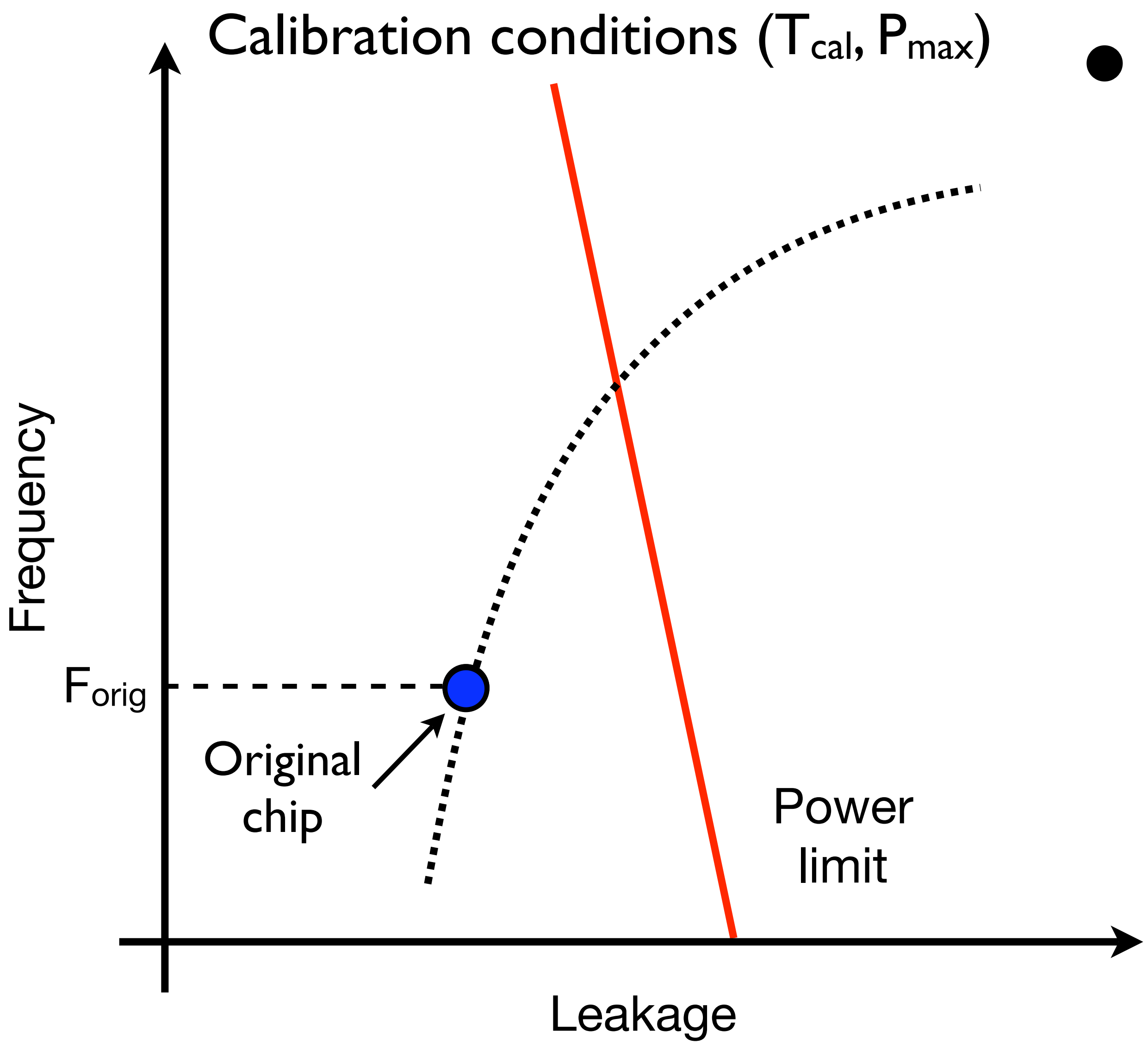


i-acoma group

Frequency binning



Calibration after manufacturing



- Calibration takes place at maximum temperature T_{cal} (burn-in oven)

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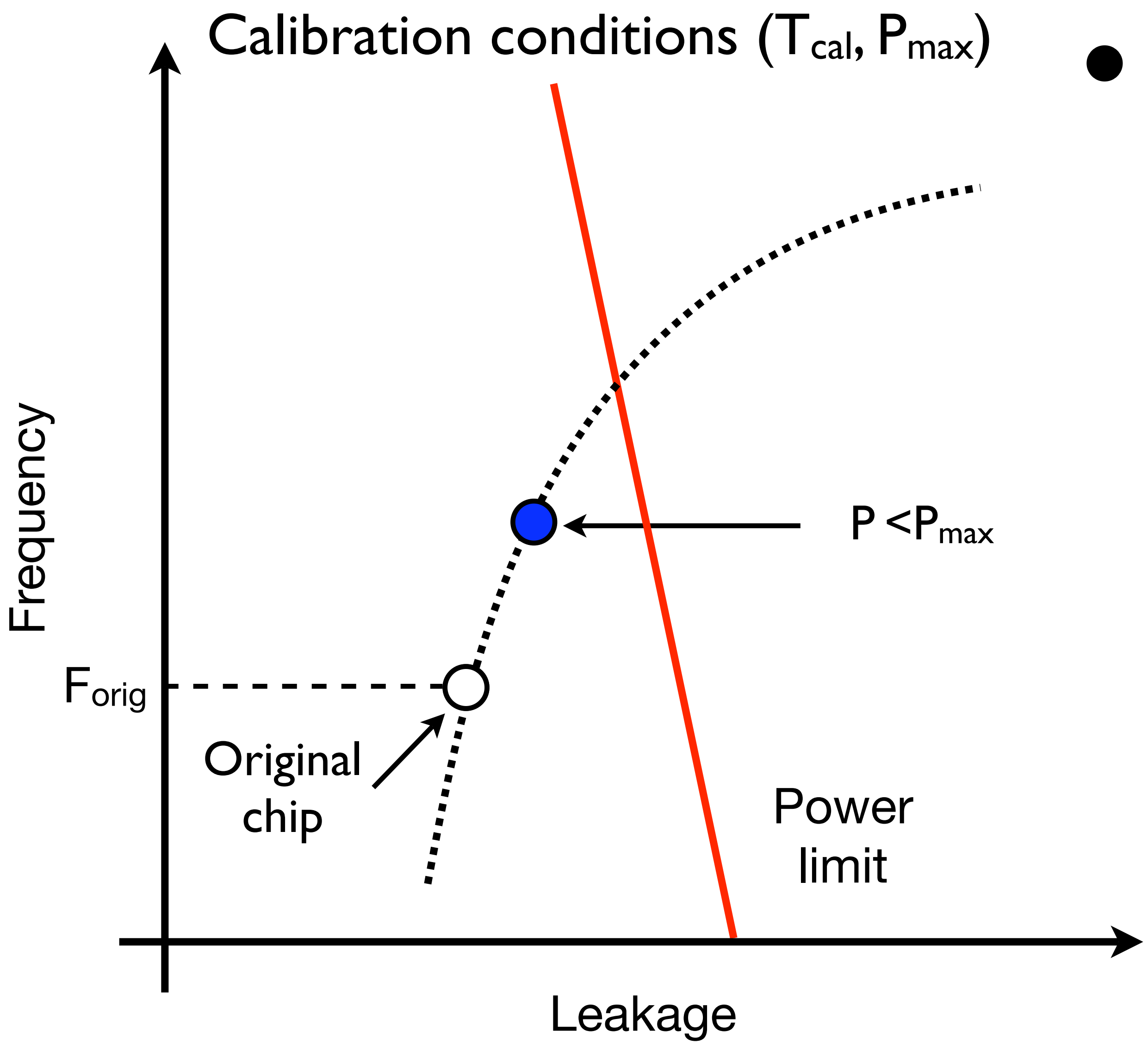

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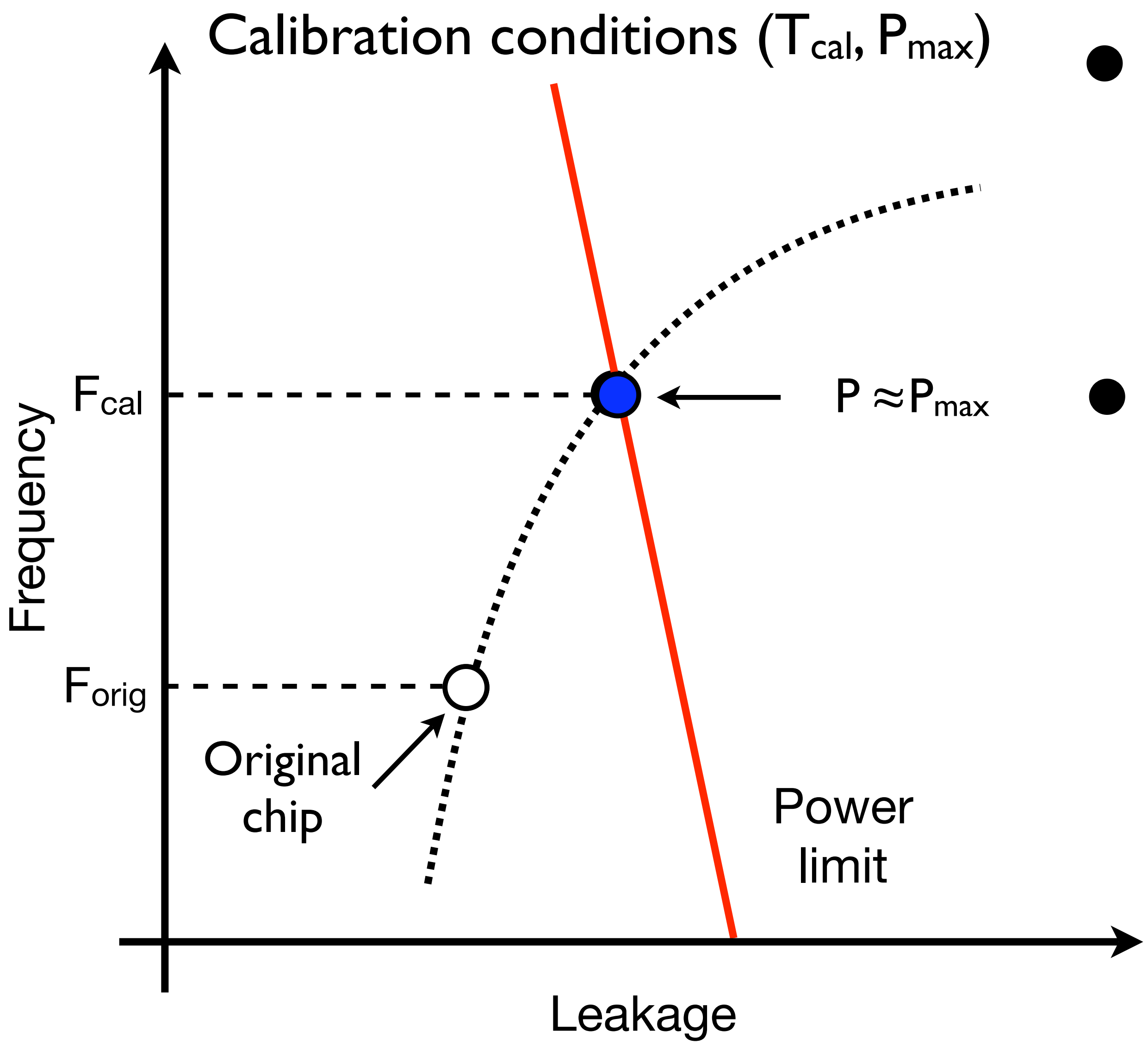

- Calibration takes place at maximum temperature T_{cal} (burn-in oven)
- F_{cal} becomes the chip's frequency

Outline

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- Dynamic fine-grain body biasing (D-FGBB)
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Motivation for D-FGBB

- Significant temperature variation:
  - Space: across different functional units, on chip
  - Time: as the activity factor of the workload changes
  - Between average and worst case conditions (T_{cal})
- D-FGBB can exploit this temperature variation
  - Adapt the body bias to changing conditions

Motivation for D-FGBB

- **Optimal** body bias:

  The body bias than **minimizes** leakage power at the target frequency

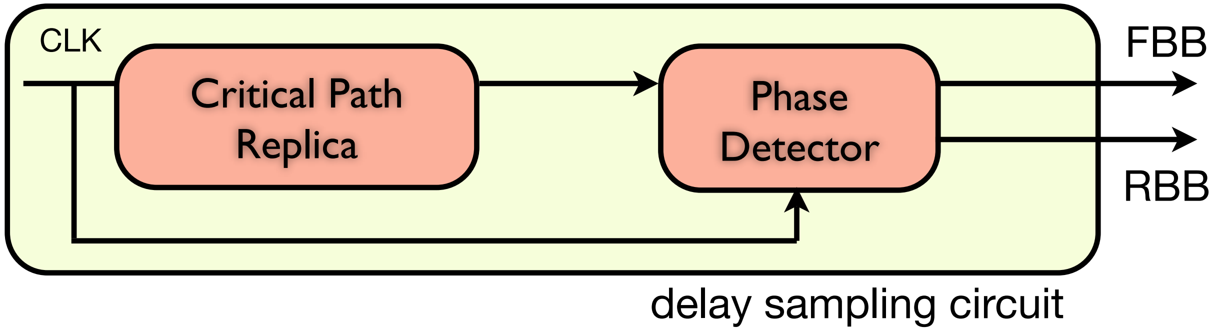
- Circuit delay changes with temperature

- Therefore optimal BB changes with temperature

The goal of D-FGBB is to keep the body bias optimal as T changes

Finding the optimal BB

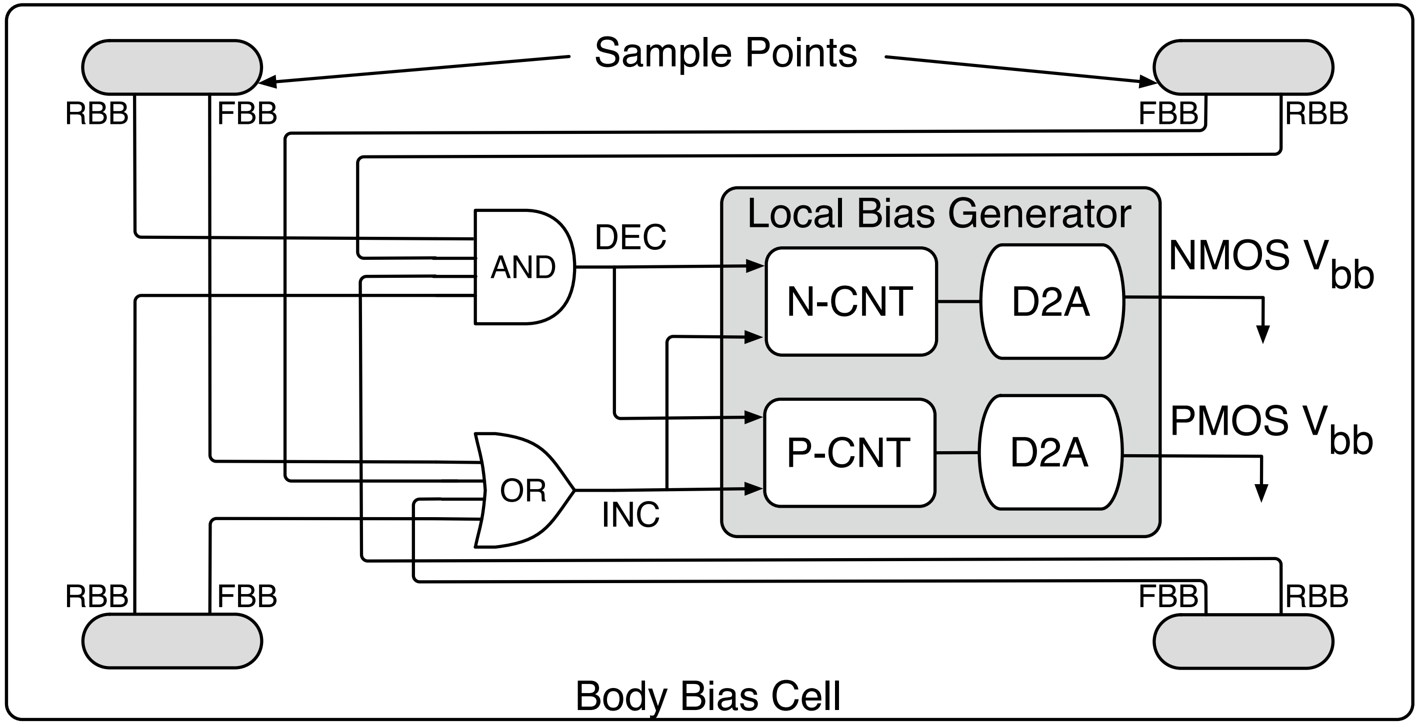
- Measure the delay of each BB domain (cell)
- Delay sampling circuit:



- Phase detector - measures delay of critical path replica
  - If slow - FBB signal raised
  - If fast - RBB signal raised

Applying dynamic fine-grain BB

- BB is determined based on feedback from delay samples



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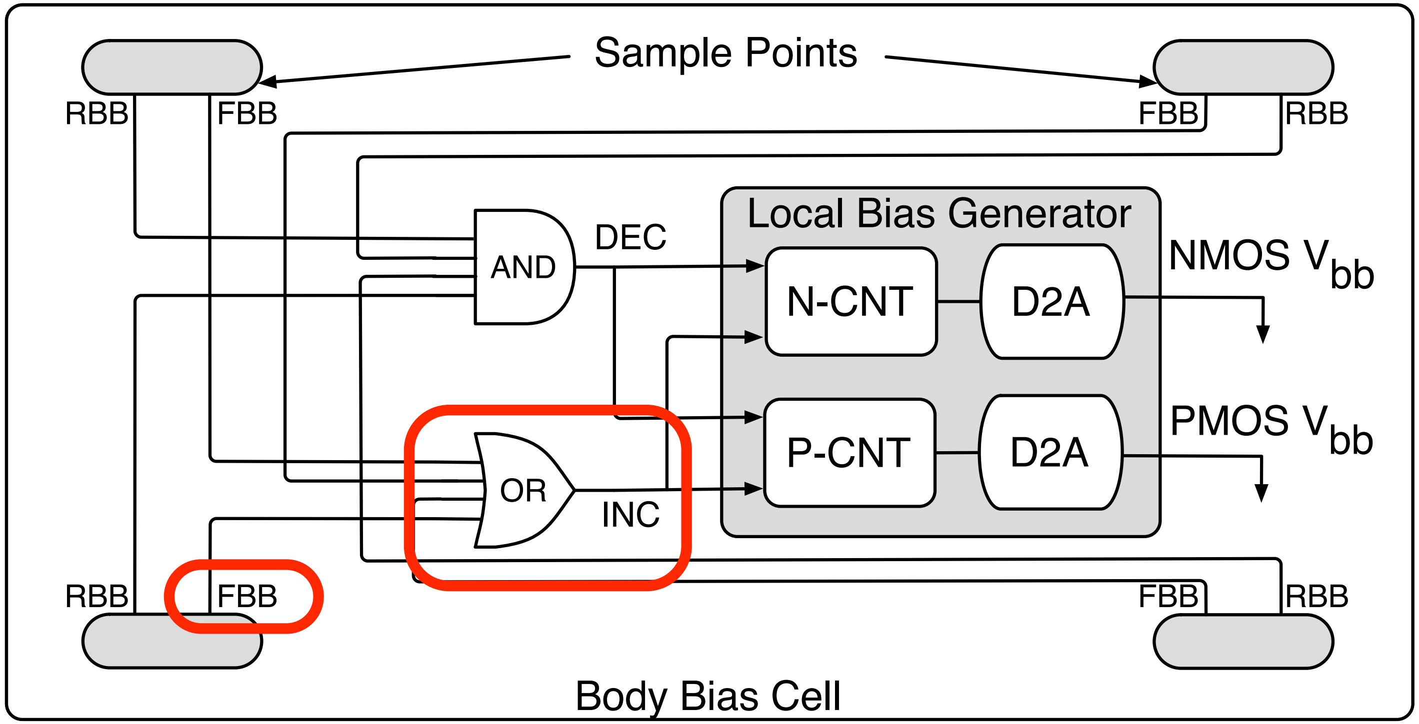

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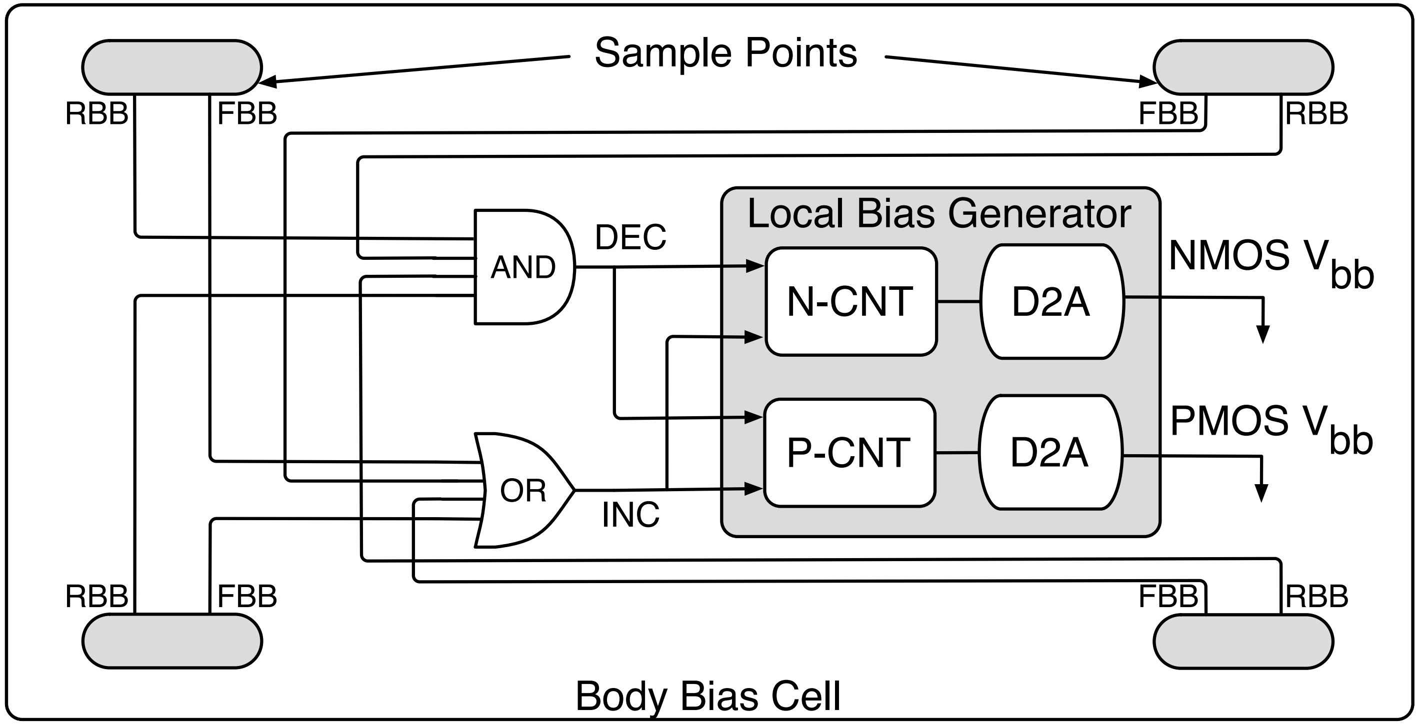

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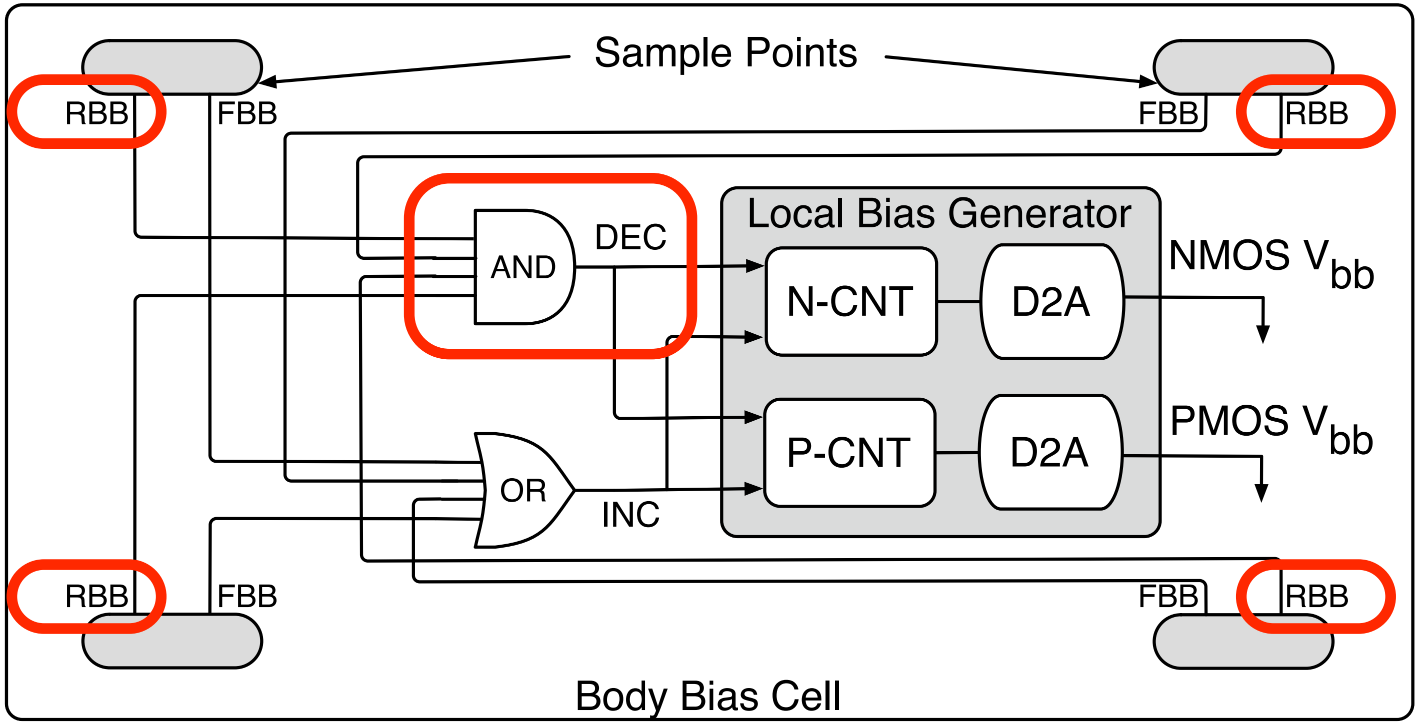

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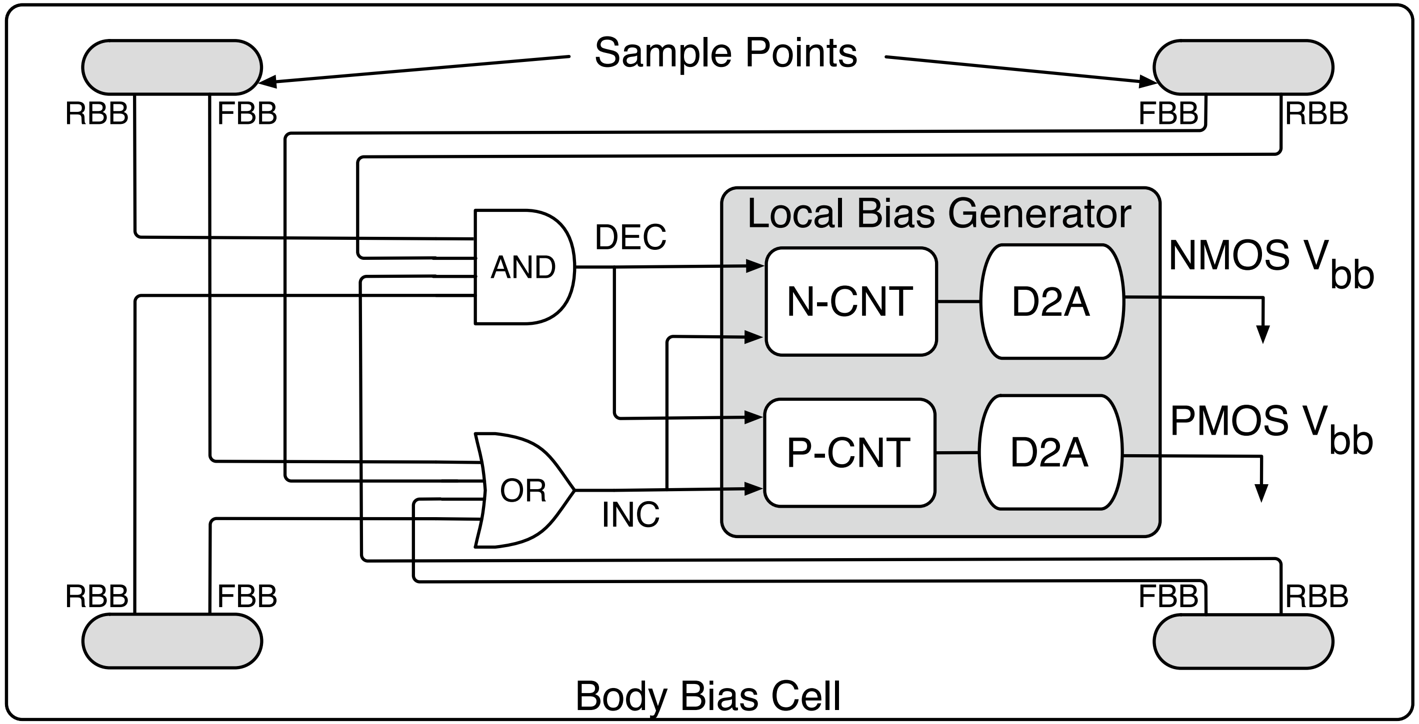

- The BB changes until optimal delay is reached
- BB stays constant, until T conditions change again

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D-FGBB environments

Operating environments	D-FGBB
Standard 	Minimize **leakage power** at F_{cal}
High performance 	Maximize **average frequency**
Low Power 	Minimize **leakage power** at F_{orig}

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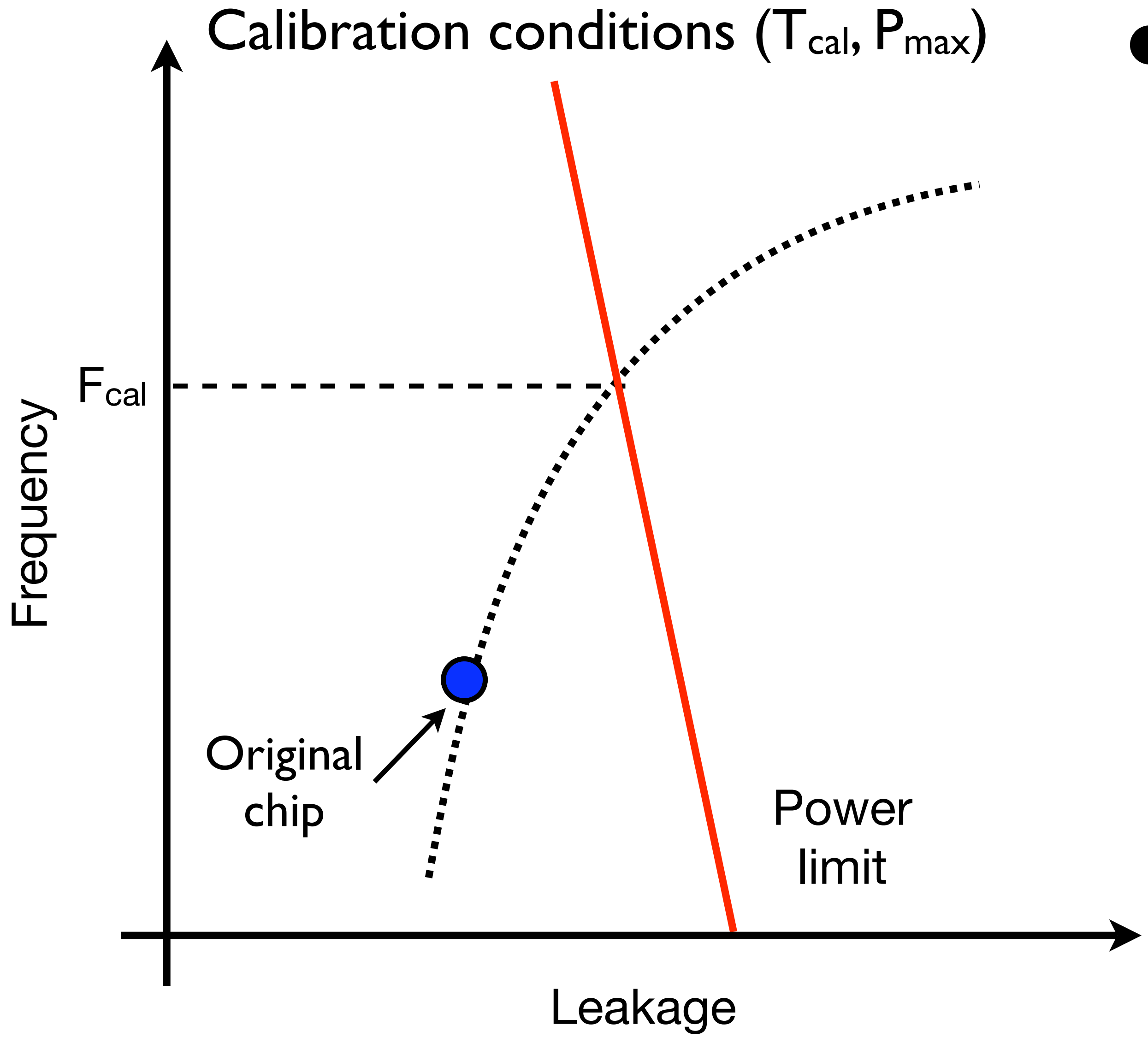
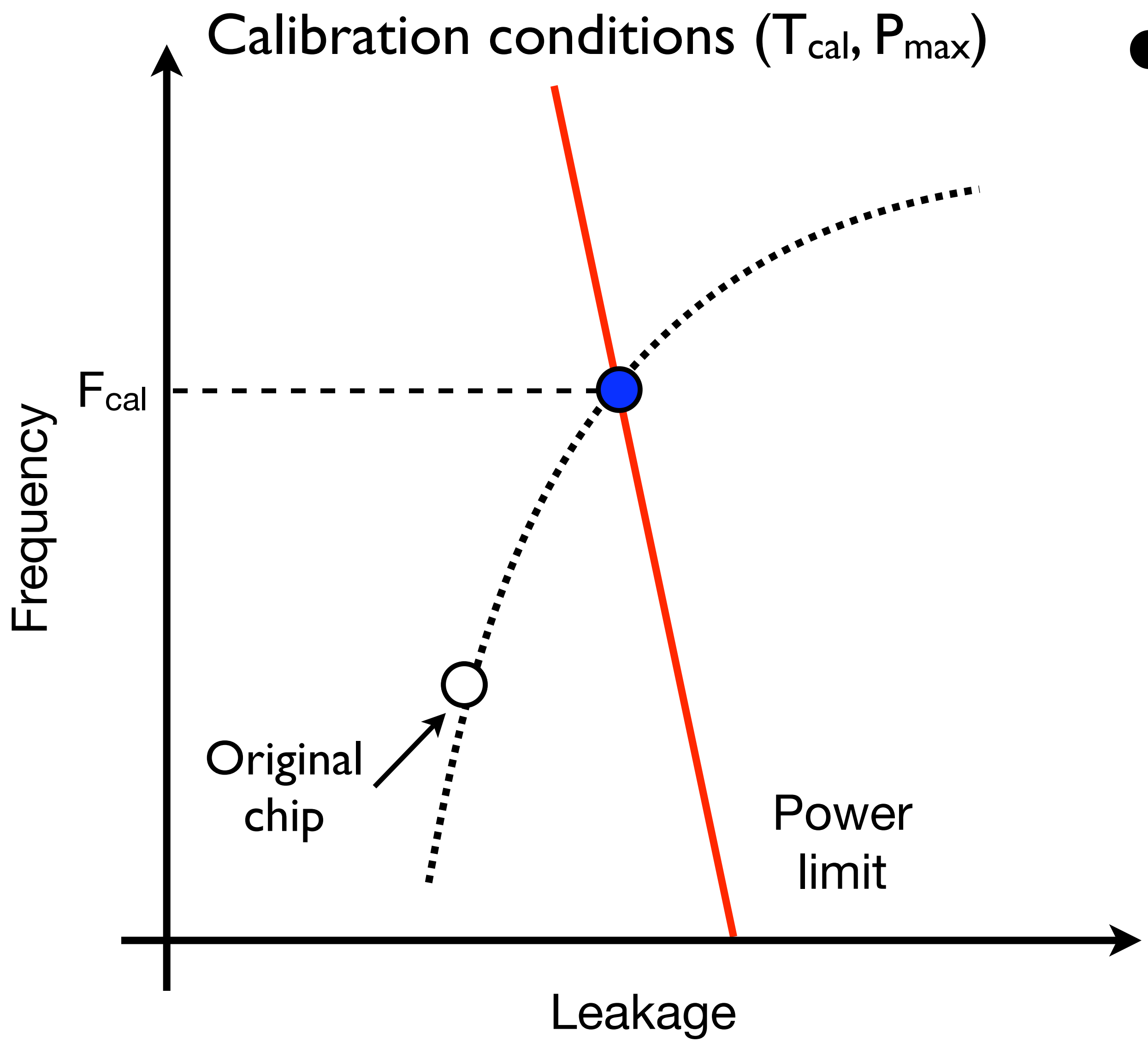


- S-FGBB finds and sets F_{cal}

Standard environment



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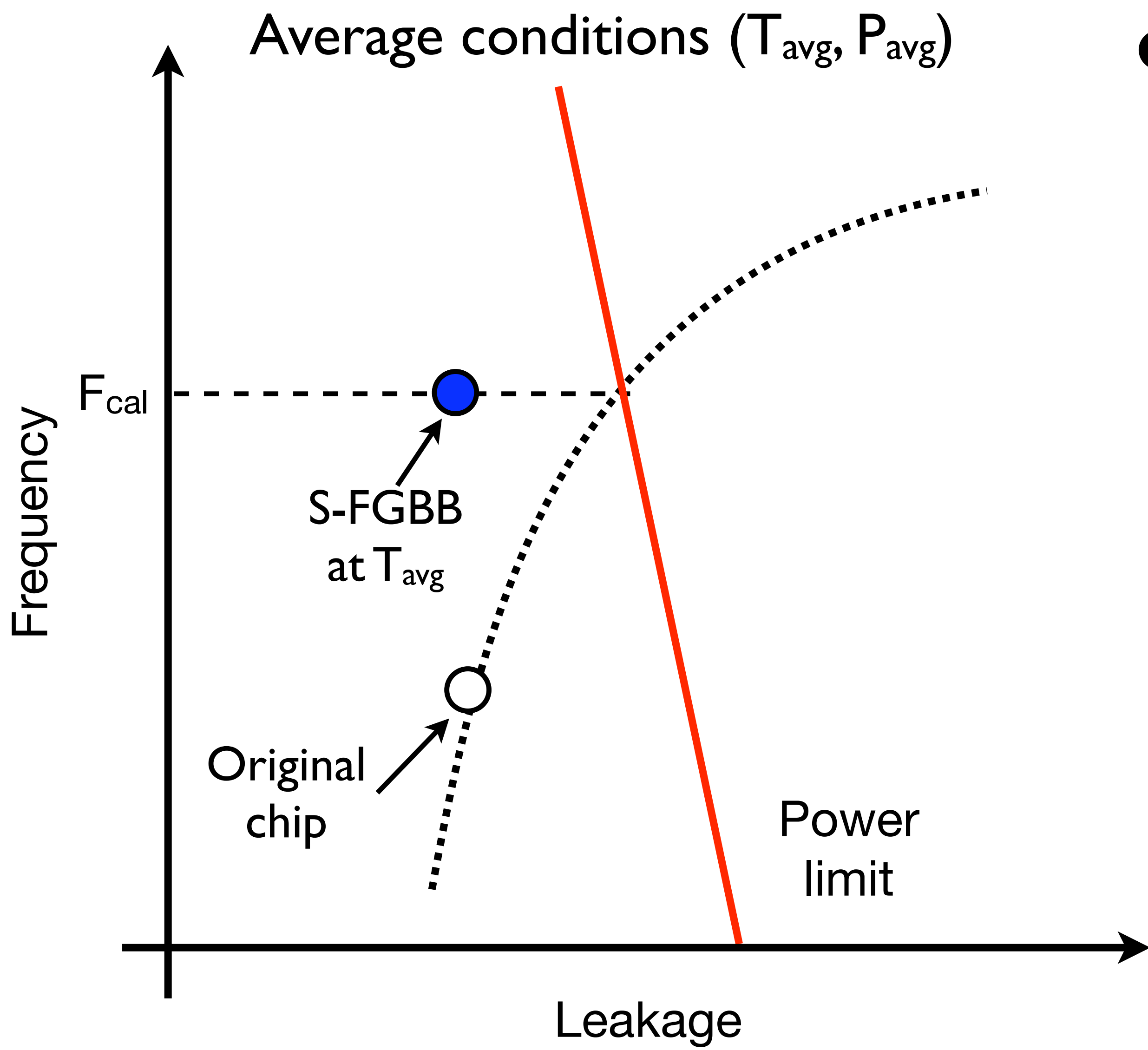

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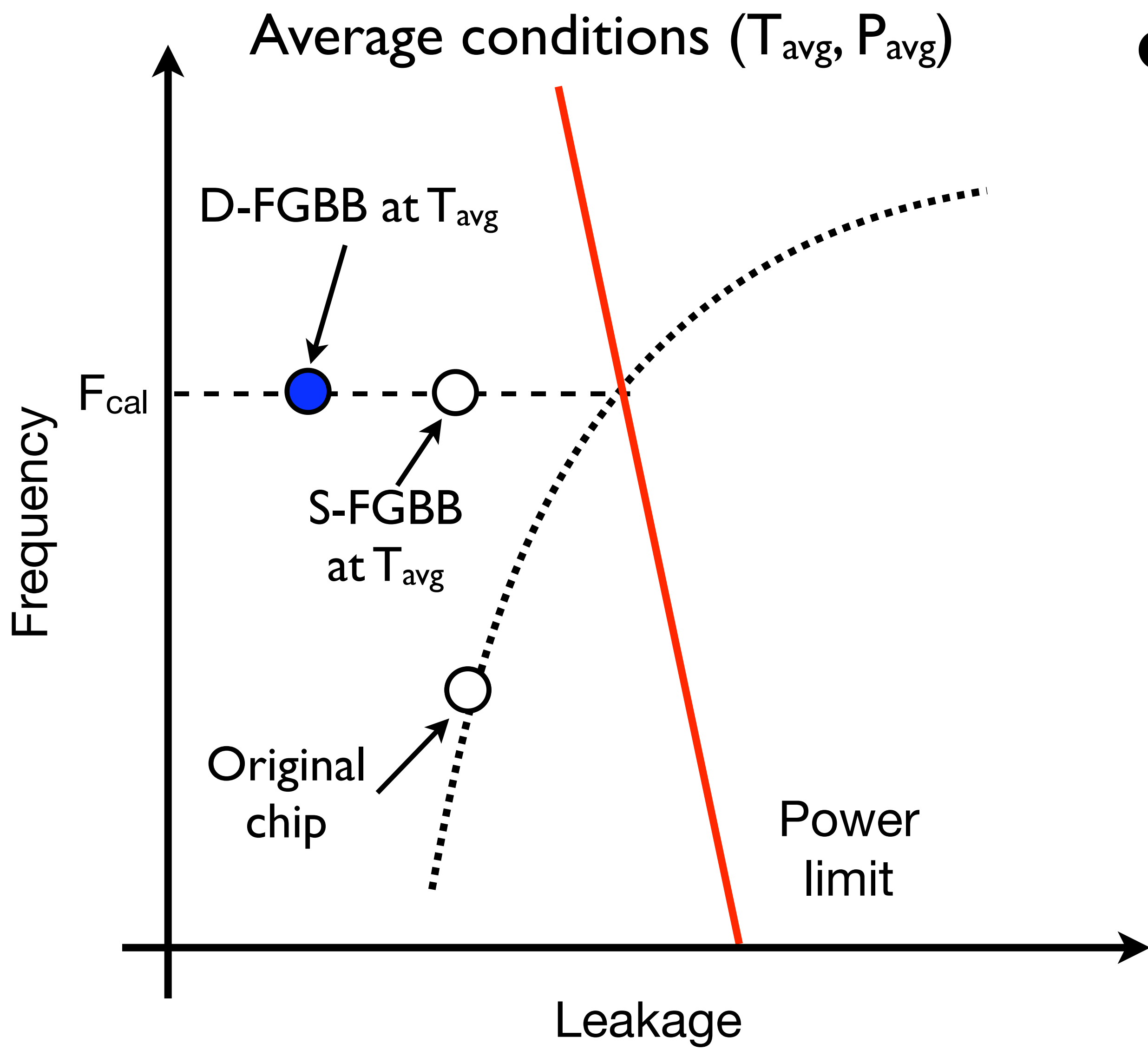

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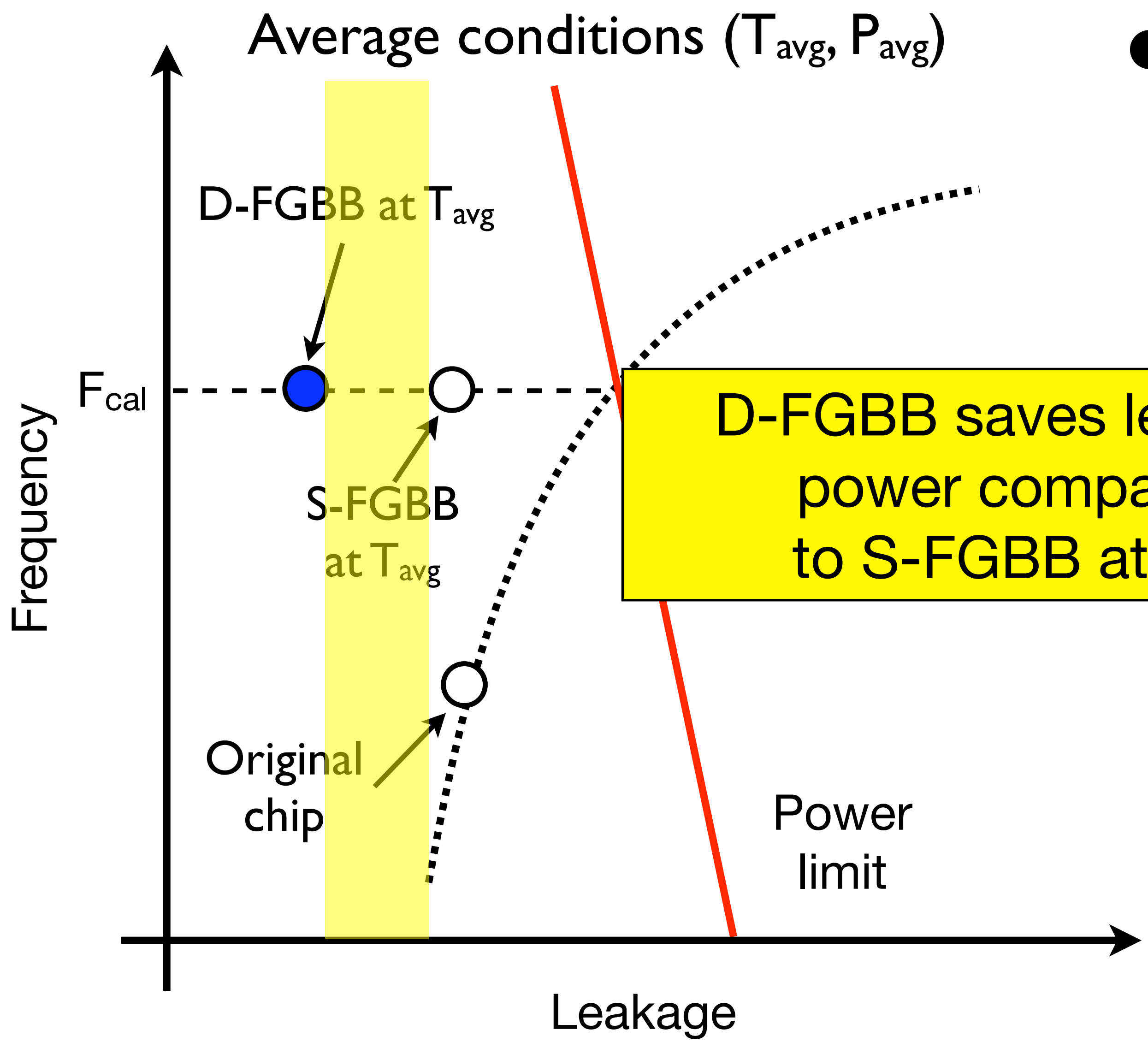

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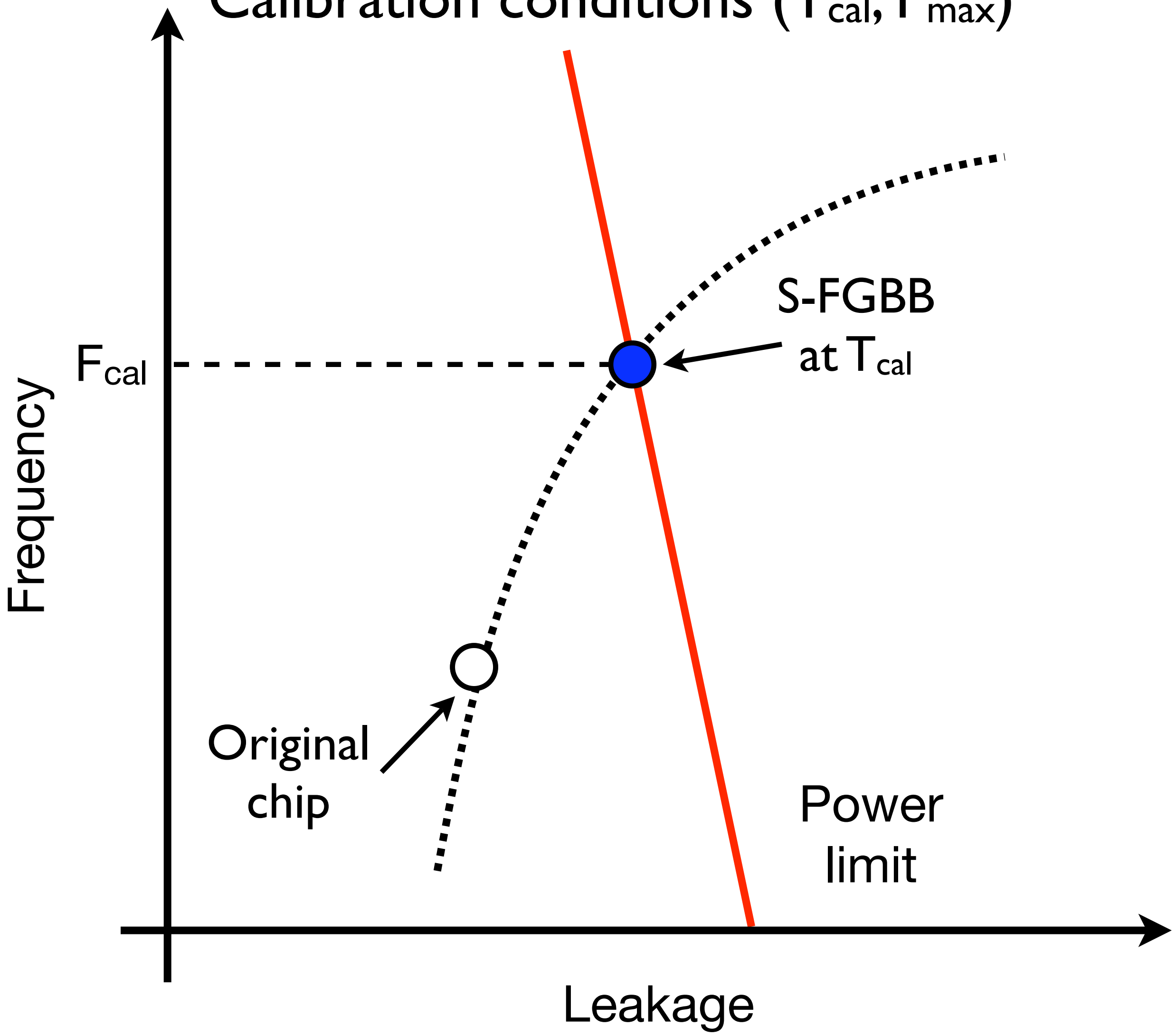
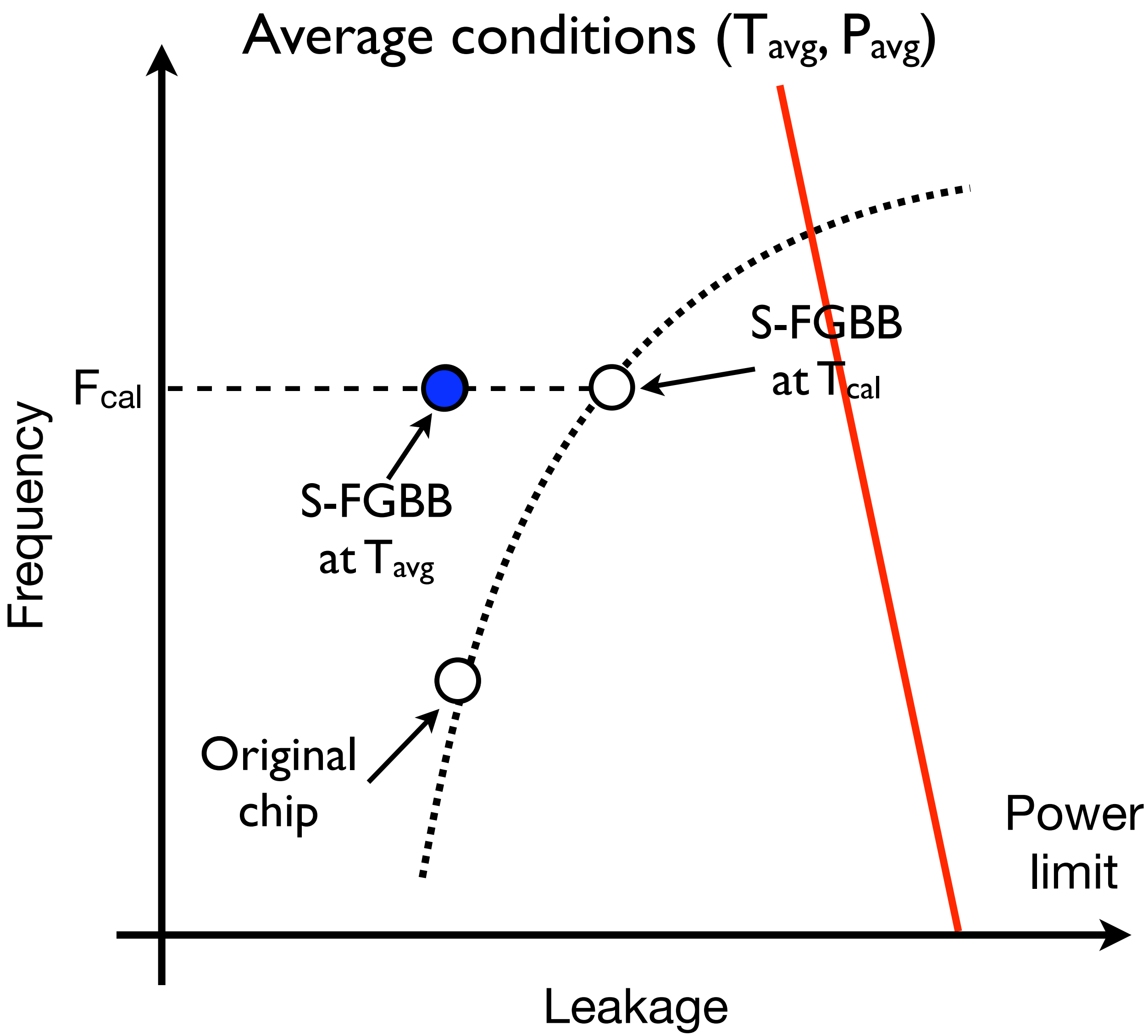
High performance

Calibration conditions (T_{cal}, P_{max})



- Average power $P_{avg} << P_{max}$

High performance



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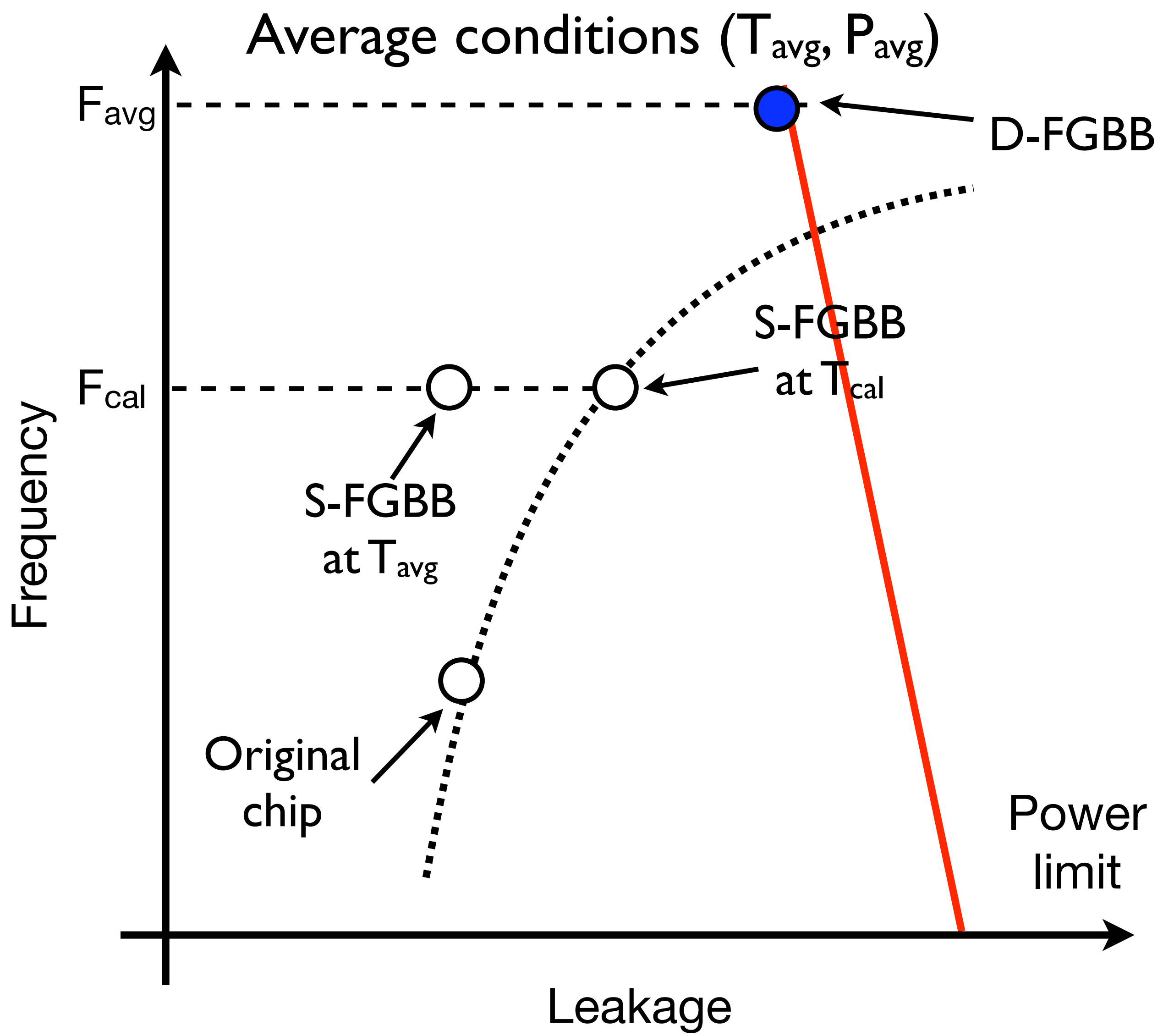

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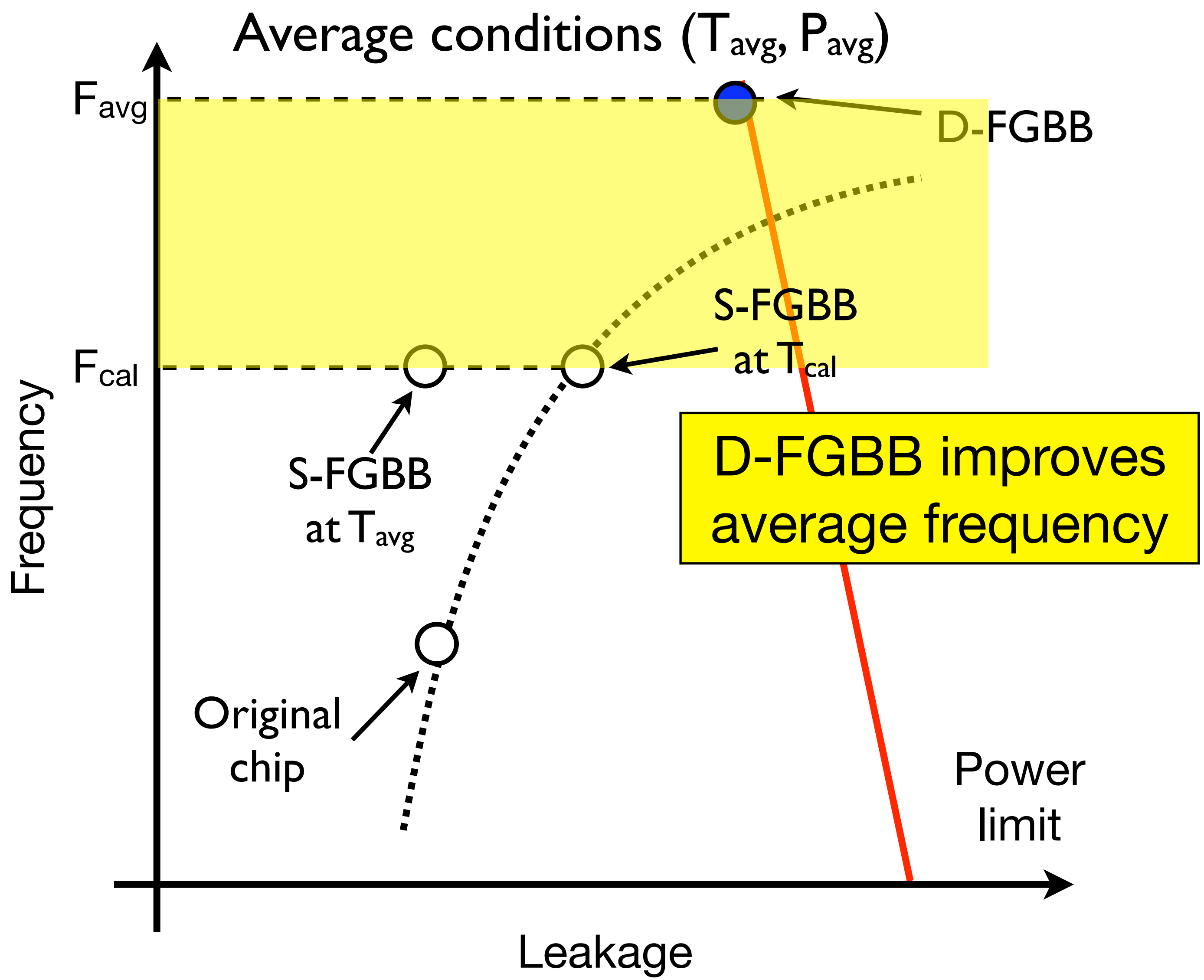

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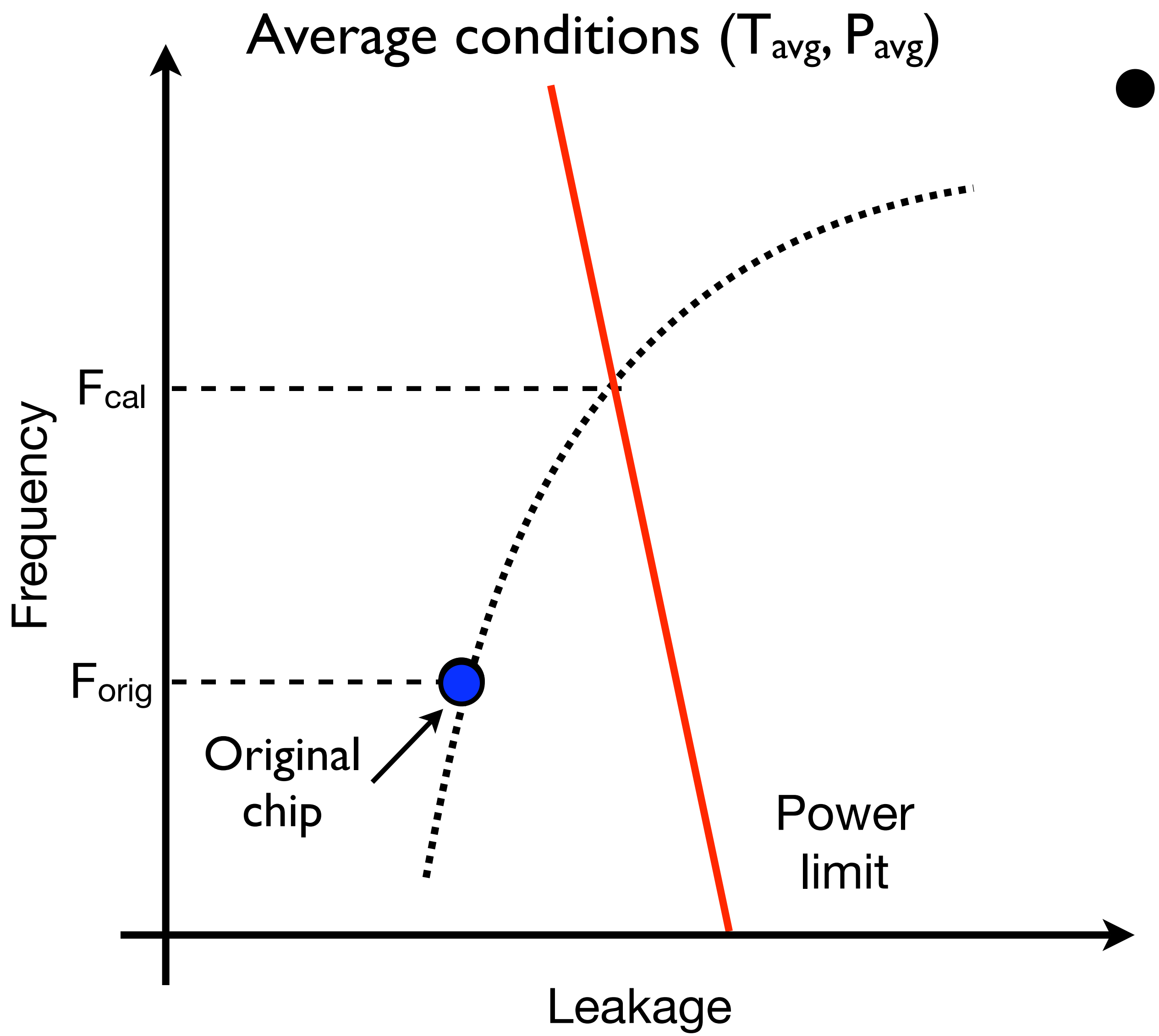
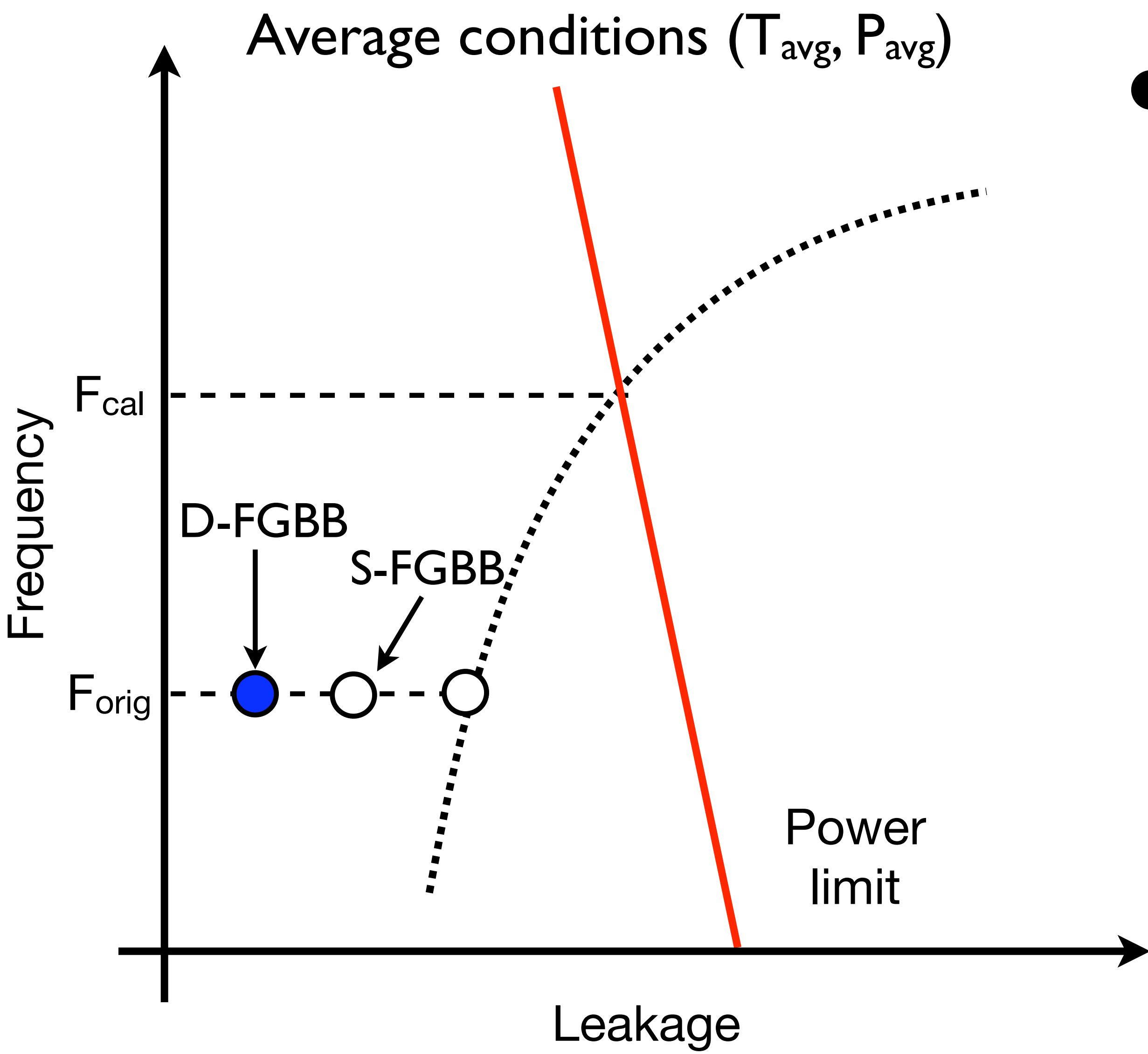
Low power



- The chip runs at its original frequency (F_{orig})

Low power



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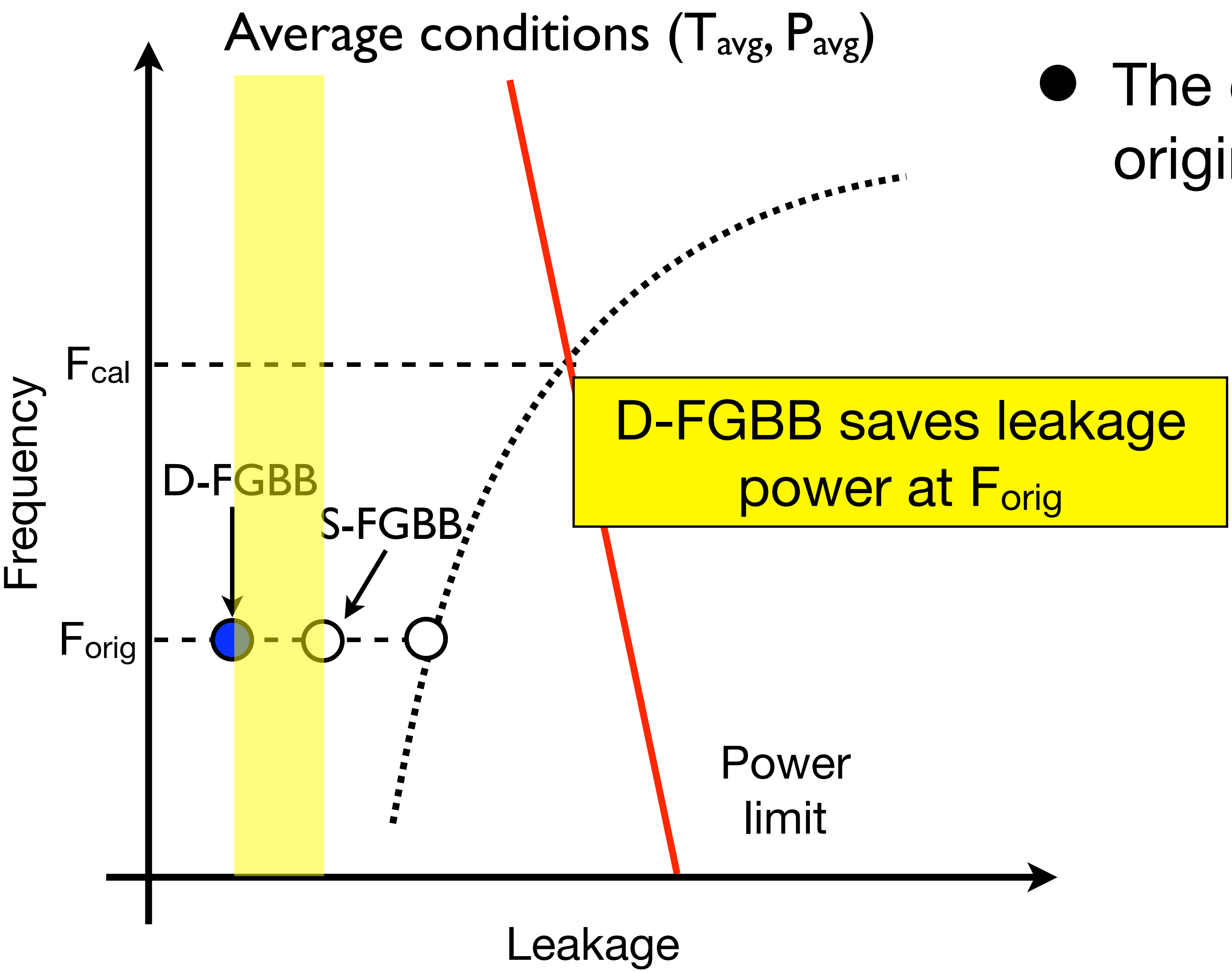

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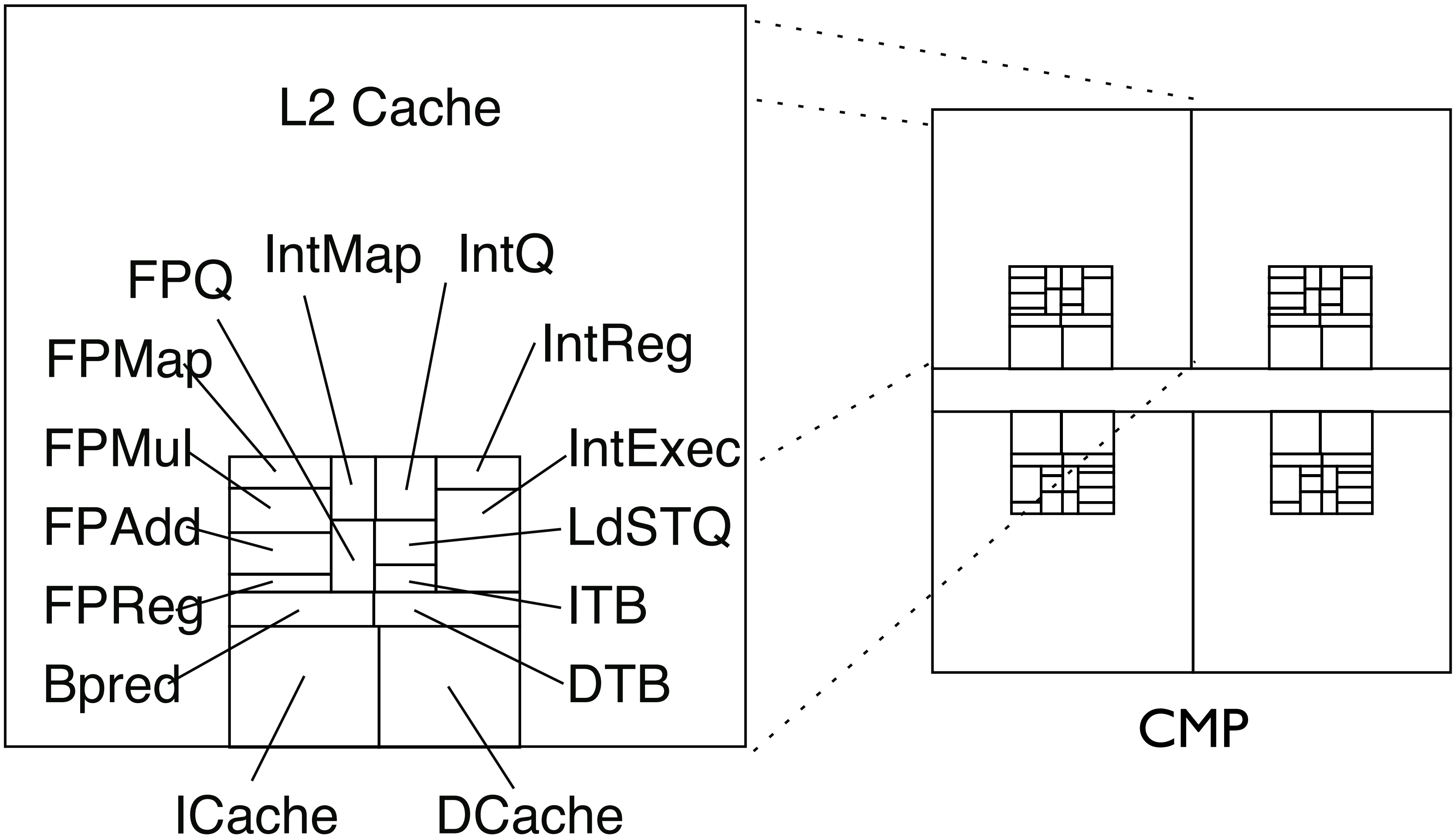
Evaluation infrastructure

- Process variation model - *VARIUS* [ASGI'07]
  - Generate V_{th} and L_{eff} variation maps for 200 chips
- SESC - cycle accurate microarchitectural simulator - execution time, dynamic power
  - Mix of SPECint and SPECfp benchmarks
- HotLeakage, SPICE model - leakage power
- Hotspot - temperature estimation

Evaluation parameters

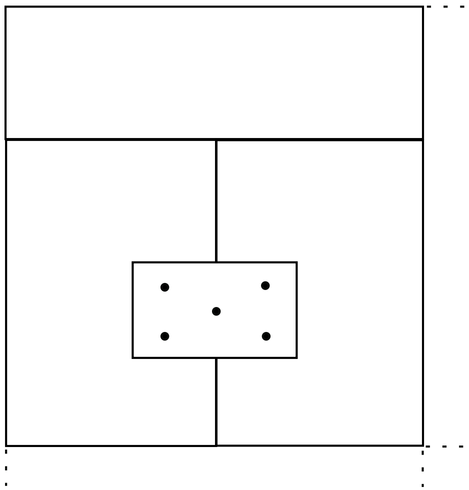
- 4-core CMP, based on Alpha 21364
- 45nm technology, 4GHz
- V_{th} variation: σ_{Vth}/μ_{Vth}=3-12%, $\sigma_{sys}=\sigma_{rand}$
- L_{eff} variation $\sigma_{Leff}= \sigma_{Vth}/2$
- V_{dd}=1V, V_{th0}=250mV, V_{bb}= ±500mV

CMP architecture

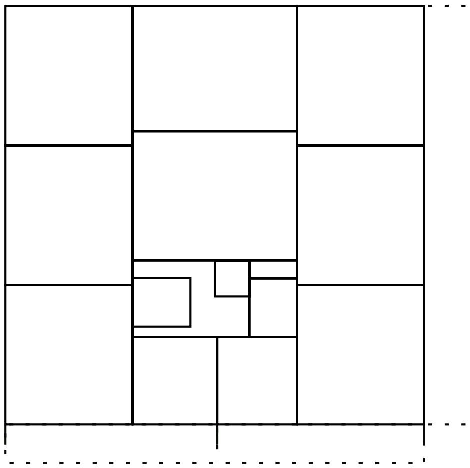


Body bias granularity

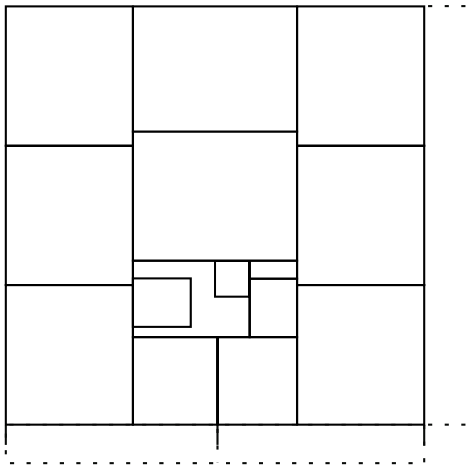
- We evaluate FGBB at different granularities
  - 1 - 144 BB cells per chip
- Shapes and sizes follow functional units



FGBB16



FGBB64



FGBB144

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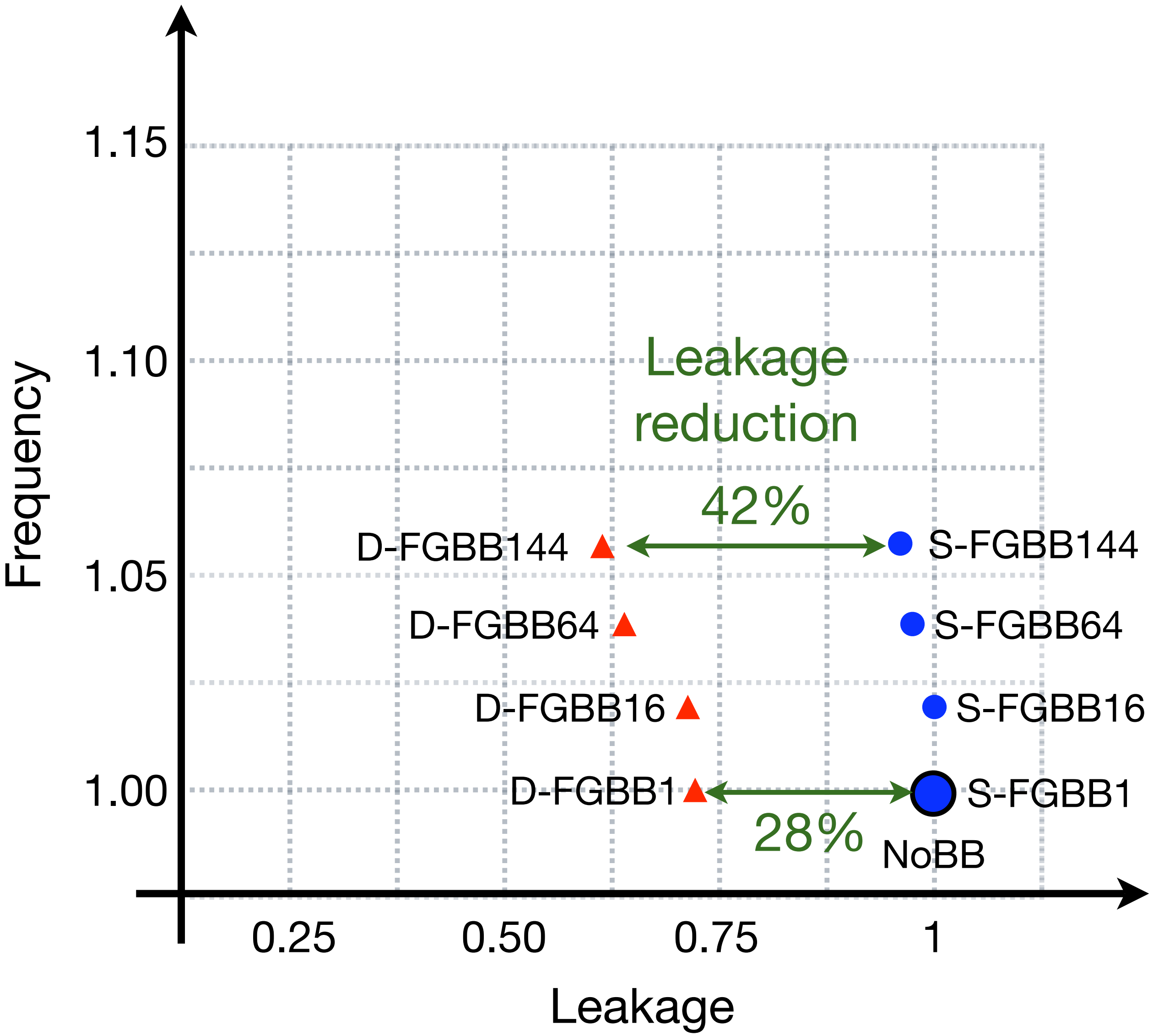
D-FGBB reduces leakage



- D-FGBB reduces leakage significantly
- More BB cells result in higher frequency and lower leakage

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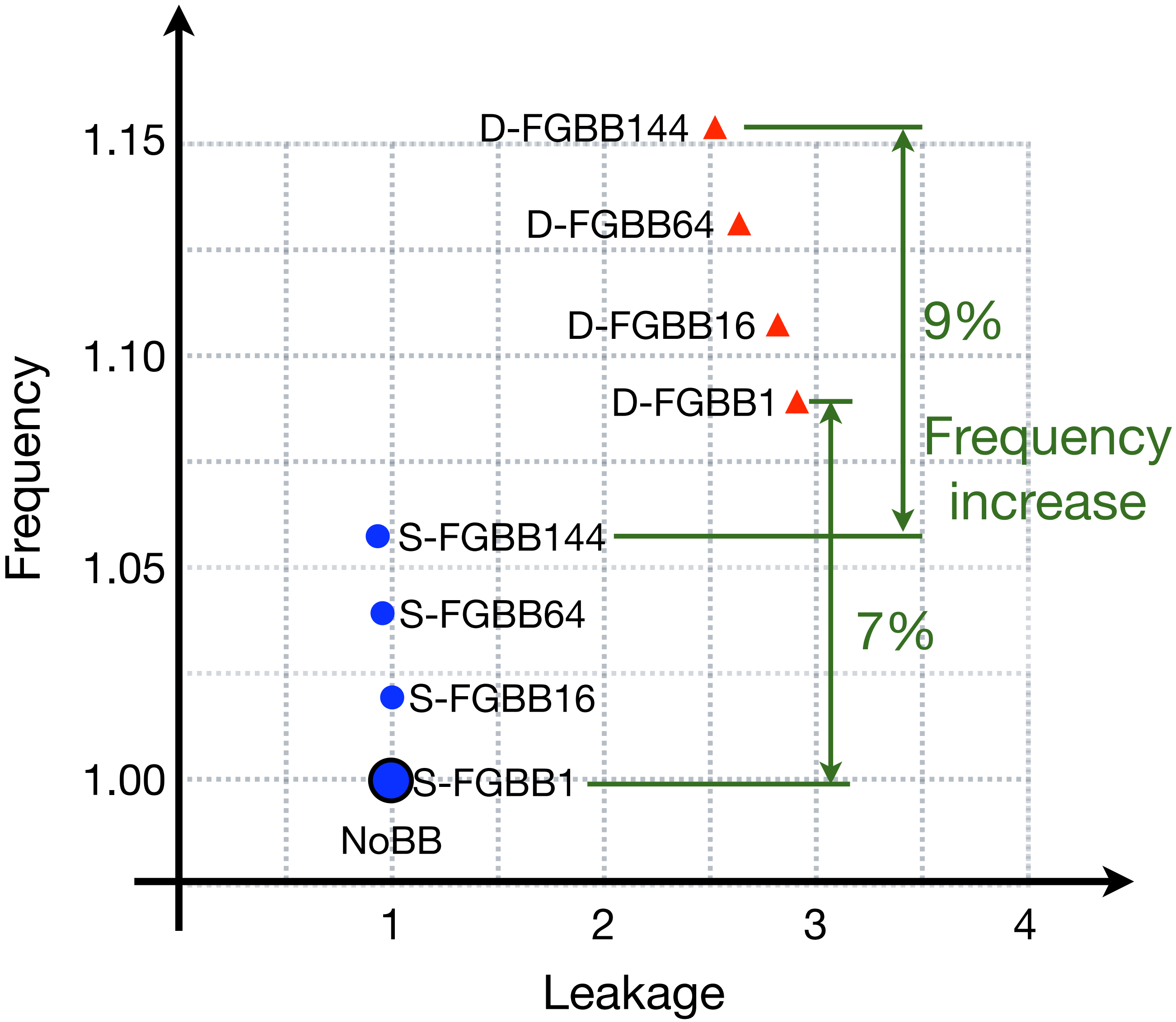
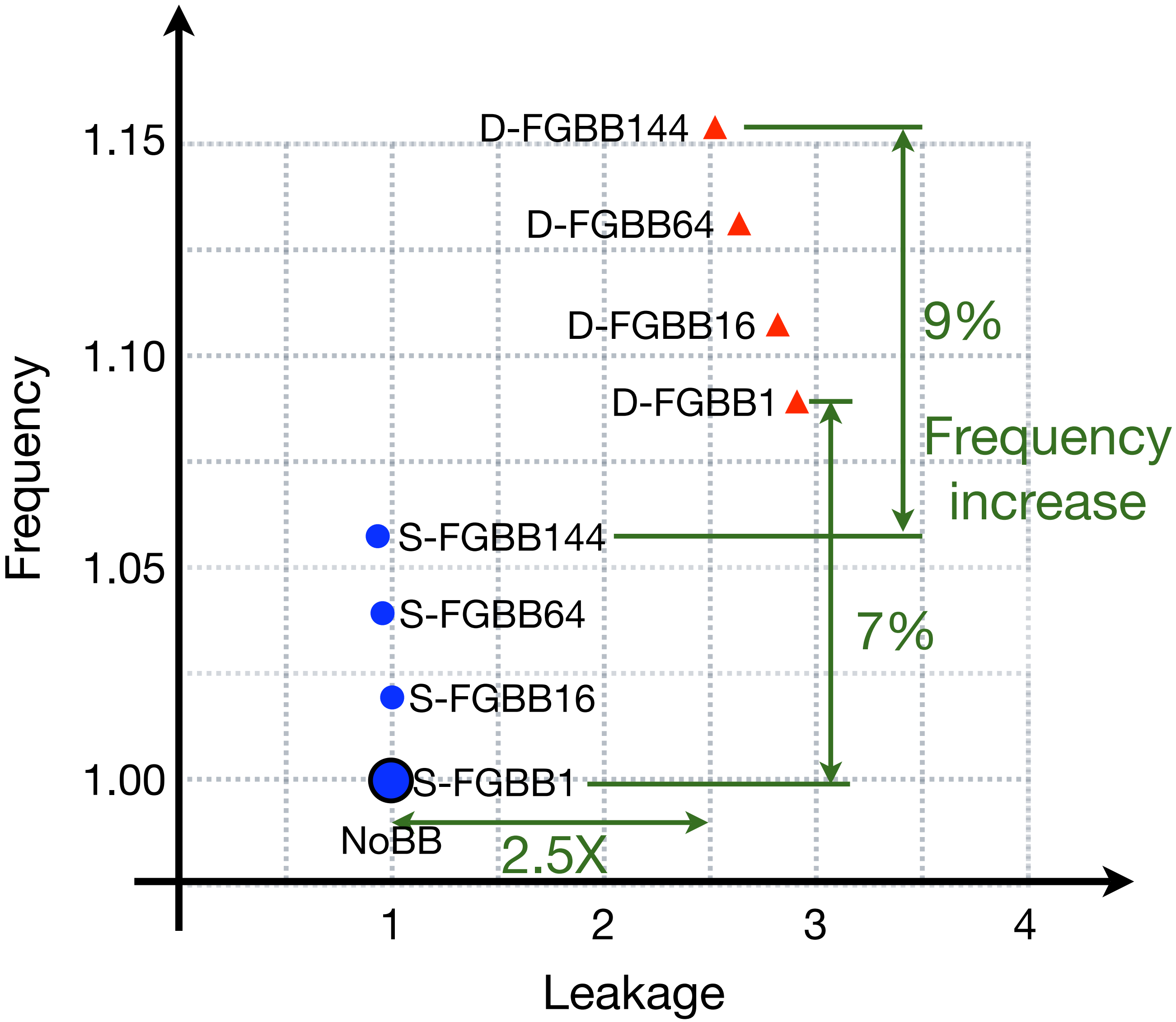
D-FGBB improves frequency



- More BB cells result in a higher increase

D-FGBB improves frequency

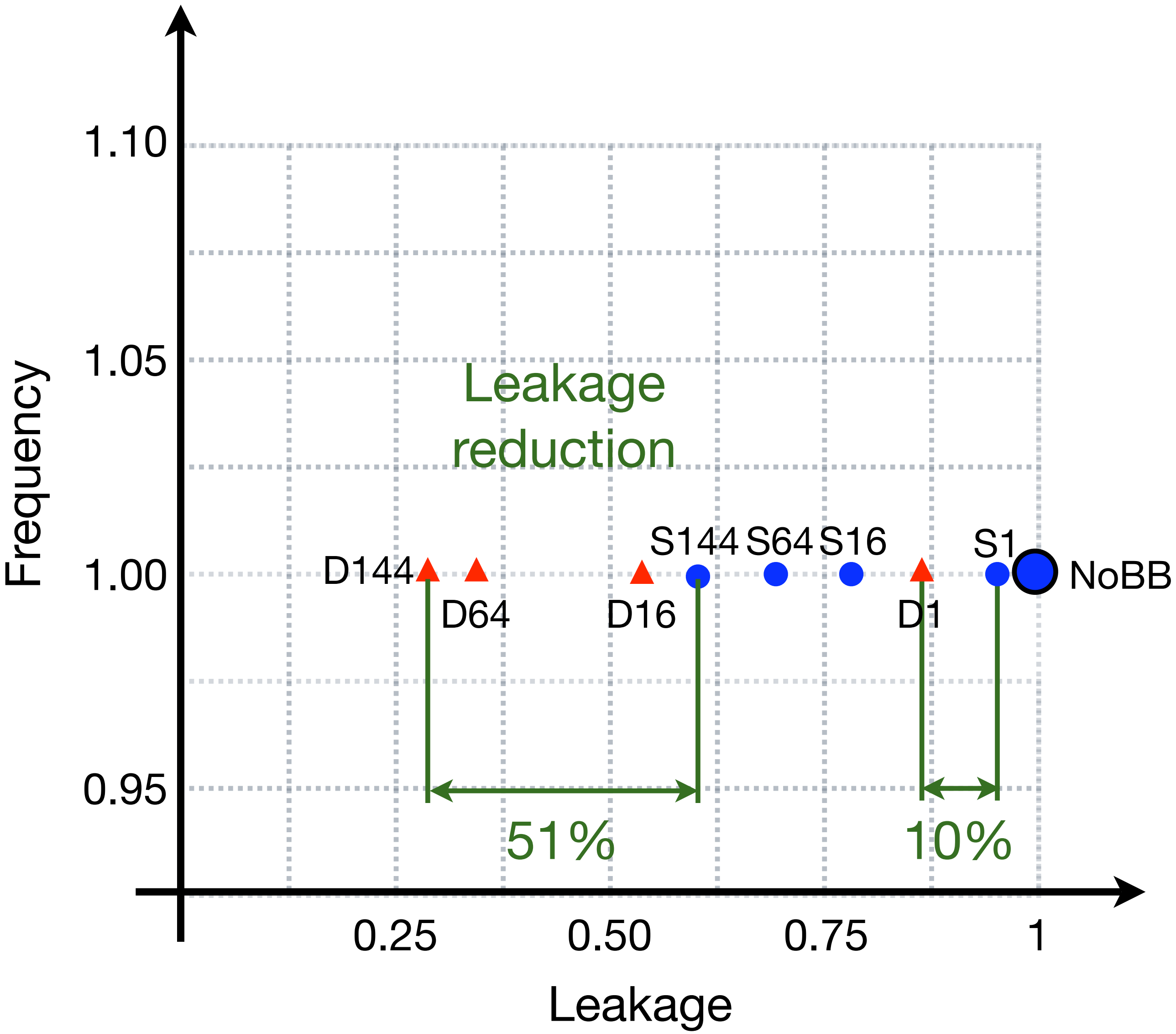


- More BB cells result in a higher increase
- Significant power cost, but still within the power budget

D-FGBB environments

Operating environments	D-FGBB
Standard 	Minimize **leakage power** at F_{cal}
High performance 	Maximize **average frequency**
Low Power 	Minimize **leakage power** at F_{orig}

D-FGBB reduces leakage



- More BB cells result in higher savings

Conclusions

- D-FGBB is more effective than S-FGBB at reducing WID variation:
  - 50% lower leakage 
  - 10% higher frequency 
  - because D-FGBB adapts to T variation
- D-FGBB can give architects an additional knob to tradeoff frequency/power

More in the paper...

- Details about our variation model
- A solution for combining D-FGBB with DVFS
- Estimated overheads of D-FGBB
- More implementation details

Mitigating Parameter Variation with Dynamic Fine-Grain Body Biasing

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