Welcome to the

Second International Workshop on Communication Architectures at Extreme Scale

(ExaComm'16)

Goals and Objectives of the Workshop

- Extreme Scale computing is marked by multiple-levels of hierarchy and heterogeneity
- Data movement is seen as the soul of different challenges for exascale computing
- Advances in networking technologies such as NoCs (like NVLink and Storm Lake), RDMA enabled networks and the like are constantly pushing the envelope of research
- Bring together researchers and software/hardware designers involved in creating network-based computing solutions for extreme scale architectures to
  - Share their experiences and
  - Learn opportunities and challenges in designing next-generation HPC systems and applications.

Thanks …..

- Authors who submitted papers
- Program Committee Members
- Keynote and Invited Speakers
- Speakers, Session Chairs, Panel Moderator, and Panelists
- Attendees

Overview of Today's Program

Start	End	Event	Speaker(s)		Organization
8:50	9:00	**Opening Remarks**			
9:00	10:00	Keynote: Optimizing Network Usage on Sequoia and Sierra	Bronis R de Supinski		LLNL
10:00	10:30	Invited Talk 1: Toward Extreme Scale: Requirements for Next-Generation Fabrics	William (Bill) Magro		Intel
10:30	11:00	Invited Talk 2: Topology-Awareness in the Tofu Interconnect Series	Yuichiro Ajima		Fujitsu, Japan
11:00	11:30	**Coffee Break**			
11:30	12:00	Invited Talk 3: Technologies for improved scaling on GPU Clusters	Jiri Kraus		NVIDIA
12:00	12:30	Invited Talk 4: BXI - The new scalable interconnect for HPC	Jean-Pierre Panziera		Bull Atos Technologies
12:30	1:00	Invited Talk 5: About Management of Exascale Systems	Tor Skeie		Simula Labs, Norway
1:00	2:00	**Lunch Break**			
2:00	2:30	Invited Talk 6: Exascale by Co-Design Architecture	Michael Kagan		Mellanox
2:30	3:00	Invited Talk 7: Next Generation Interconnection for Accelerated Computing	Taisuke Boku		University of Tsukuba, Japan
3:00	4:00	Research Paper Session SONAR: Automated Communication Characterization for HPC Applications Reducing the overhead of manipulating data-structure on PGAS by ordering memory access at the remote-side	Steffen Lammel Yuichiro Ajima		University of Heidelberg, Germany Fujitsu, Japan
4:00	4:30	**Coffee Break**			
4:30	6:00	Panel: Beyond Speeds and Feeds - What New Capabilities Are Needed for Exascale Interconnects?	Moderator	Ron Brightwell	Sandia
			Panelists	Jeff Hammond Daniel Holmes Laxmikant V. Kale Jay Lofstead Tor Skeie	Intel EPCC UIUC Sandia Simula
6:00	6:10	**Closing Remarks**			

Some Guidelines

- Let’s try to achieve a true workshop style interaction
  - Questions and discussions for each presentation
  - Keep time constraints in mind
  - Longer discussions can be done during the break/lunch time
- Speakers can check their laptops and presentations in advance (during the break)

Final Thanks …

- Bernd Mohr and Michela Taufer
  - Workshop Co-Chairs
- Julian Kunkel
  - Proceedings Chair
- Heike Walther
  - Conference Program Coordinator