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Buckeye Alumni Creating Knowledge

A CSE Department Colloquium Series

Who: DANA VANTREASE (UNIVERSITY OF WISCONSIN)

What: Under Pressure: Register Files in Multithreaded Processors

When: MON, APR 11, 5:00 PM, IN DL 480; PIZZA AFTERWARD!

The relentless demand for higher performance processors drives designers to increase the pipeline depth, grow the issue width, and provide multithreaded support. All of these techniques demand large physical register files. However, the access time of a register file is directly affected by its size, and the delay incurred by large register files is detrimental to performance.

In this talk, I will discuss the evolution of the register file architecture and present several solutions to cope with register file access-latency. Additionally, I will present a technique called Physical Register Inlining (PRI) as applied to simultaneous multithreaded architectures. PRI advocates efficiently utilizing the physical register file, rather than enlarging its capacity by exploiting the register rename table whenever possible. Specifically, when a register value can be expressed with fewer bits than the register map would need to specify a physical register number, the value is stored directly in the map, avoiding indirection, and saving space in the physical register file. Basic knowledge of computer architecture is recommended, but not required, for this talk.

Dana Vantrease is a graduate student in the PHARM group in the Department of Computer Science at the University of Wisconsin-Madison. She received a BS in computer science and engineering from the Ohio State University in 2002. Dana is a recipient of the 2004 NSF Graduate Research Fellowship. While in graduate school, her research has focused on simultaneous multithreaded architectures, coping with non-deterministic execution, and soft-error tolerance.

Contact and host: Prof. Bruce W. Weide (weide.1@osu.edu).