1. D is true iff a majority of inputs is low, i.e. at least two out of the three inputs is low. So the function for D is:
\[ D = \overline{A} \overline{B} + \overline{B} \overline{C} + \overline{A} \overline{C} \]

a) Input bubble form:

b) \[ D = \overline{A} \overline{B} + \overline{B} \overline{C} + \overline{A} \overline{C} = \overline{A} f_0(B, C) + A f_1(B, C) \]
\[ f_0(B, C) = \overline{B} + \overline{B} \overline{C} + \overline{1} \overline{C} = \overline{B} + \overline{C} + \overline{B} \overline{C} = \overline{B} + \overline{C} \]
\[ f_1(B, C) = 0 \overline{B} + \overline{B} \overline{C} + 0 \overline{C} = \overline{B} \overline{C} \]

\[ \overline{B} + \overline{C} = \overline{B} \cdot 1 + \overline{B} \cdot \overline{C} \] and \[ \overline{B} \overline{C} = \overline{B} \cdot \overline{C} + \overline{B} \cdot 0 \]

So the complete circuit is:
Implementing \( f \) directly with restoring logic would require:

3 transistors each for \( n \)-logic \& \( p \)-logic (one each for \( \overline{A}, \overline{B}, \overline{C} \)) and 3 inverters to form \( \overline{A}, \overline{B}, \overline{C} \). So we will need 12 transistors.

Instead, let us consider \( \overline{f} = \overline{A} \overline{B} + \overline{A} \overline{C} \) (from the K-map)
\[ = \overline{A} (\overline{B} + \overline{C}) \]

This will require no inverters for inputs:

\[ f = A + BC = \overline{A} \cdot (0+BC) + A \cdot (1+BC) \]
\[ = \overline{A} \cdot (BC) + A \cdot 1 \]

\[ BC = \overline{B} \cdot (0 \cdot C) + B \cdot (1 \cdot C) = \overline{B} \cdot 0 + B \cdot C \]

Total \# transistors: \( 4 \) (inverters for \( A \) and \( B \)) \( + 6 = 10 \)
a) Circuit is well formed since the p-logic and n-logic are duals of each other. Considering the p-logic, which can be viewed in terms of the equivalent input bubble form (AND = series; OR = parallel):

\[ f = A \cdot (\overline{A} + B) + B \cdot (\overline{A} + \overline{B}) = A \overline{A} + A \overline{B} + B \overline{A} + B \overline{B} = A \overline{B} + \overline{A} B \]

b) This circuit is not in the standard restoring logic form (series-parallel structures). The transistors driven by C create the non-series-parallel structure. So, we can reason about two cases: C=0 and C=1.

Considering C=0, we have:

\[ f = (\overline{A} + \overline{B}) \cdot (\overline{E} \cdot D + \overline{E} \cdot (G+H)) = \overline{A} \cdot \overline{D} \cdot E + \overline{B} \cdot \overline{E} \cdot \overline{D} + \overline{A} \cdot \overline{E} \cdot (G+H) + \overline{B} \cdot \overline{E} \cdot (G+H) \]

\[ = \overline{A} \overline{D} \cdot E (E+G+H) + \overline{B} \overline{E} \cdot (G+H) \]

\[ \frac{f}{p-\text{logic implements}} \]

\[ \frac{f = A \cdot (D+E) + B \cdot (E + GH)}{n-\text{logic implements}} \]

\[ f = A \cdot (D+E) + B \cdot (E + GH) = \overline{A} \cdot \overline{D} \cdot E \cdot (E+G+H) + \overline{B} \cdot \overline{E} \cdot (G+H) \]

The two functions are not the same; for example with A=1, B=1, C=0
D=0, E=0, F=0, G=0, H=0: p-logic implements \( f = 0 \) & n-logic implements \( f \neq 0 \)
c) Circuit has p-logic connecting output to ground and n-logic connecting output to Vdd. Thus, although the circuits for the n-logic and p-logic are duals of each other (and thus implement the same function), the circuit is not well formed.

d) p-logic implements \( f = (\overline{A} + B) \cdot (\overline{E} + \overline{D}) = \overline{A}E + \overline{B}E + \overline{A}D + \overline{B}D \)

n-logic implements \( f = \frac{\overline{A}E + \overline{B}D}{(AC) \cdot (BD)} = (\overline{A} + \overline{E}) \cdot (\overline{B} + \overline{D}) \)

\( = \overline{A} \overline{B} + \overline{A} \overline{D} + \overline{B} \overline{E} + \overline{C} \overline{D} \)

The two functions are not the same: for example, with \( A=1, B=1, C=0, D=0 \), p-logic implements \( f=0 \), while n-logic implements \( f=1 \). So the circuit is not well formed.

e) The circuit is not well formed because the two C-switches are controlled by different input variables. For example, when \( B=1, C=1, A=1, D=0 \), the output will be undefined (connected to D and A, i.e. both \( a=0 \) and \( a=1 \)).

f) This is also not well formed because \( B \) and \( C \) control the two switches connected together. For example, Out is not well defined when \( A=1, B=0, C=0 \) (there is no conducting path from 0 or 1 to Out).