Compiler-Assisted Dynamic Scheduling for Effective Parallelization of Loop Nests on Multi-core Processors

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Introduction

- Ubiquity of multi-core processors
- Need to utilize parallel computing power efficiently
- Automatic parallelization of regular scientific programs on multi-core systems
  - Polyhedral Compiler Frameworks
- Support from compile-time and run-time systems required for parallel application development
for (i=1; i<=7; i++)
    for (j=2; j<=6; j++)
        S1: \( a[i][j] = a[j][i] + a[i][j-1]; \)

\[ \mathbb{F}_{3a}(x_{S1}) = \begin{pmatrix} 1 & 0 \\ 0 & 1 \end{pmatrix} \cdot \begin{pmatrix} i \\ j \end{pmatrix} + \begin{pmatrix} 0 \\ -1 \end{pmatrix} \]

\[ D_{S1}(x_{S1}) = \begin{pmatrix} 1 & 0 & -1 \\ -1 & 0 & 7 \\ 0 & 1 & -2 \\ 0 & -1 & 6 \end{pmatrix} \cdot \begin{pmatrix} i \\ j \\ 1 \end{pmatrix} \geq 0 \]
for (i=1; i<=7; i++)
for (j=2; j<=6; j++)
    S1: a[i][j] = a[j][i] + a[i][j-1];

Dependence Polytope
An instance of statement t (i_t) depends on an instance of statement s (i_s)
- i_s is a valid point in D_s
- i_t is a valid point in D_t
- i_s executed before i_t
- Access same memory location
- h-transform: relates target instance to source instance involved in last conflicting access

\[
\begin{pmatrix}
D_s & 0 \\
0 & D_t
\end{pmatrix}
\begin{pmatrix}
i_s \\
i_t
\end{pmatrix}
\geq \begin{pmatrix}
0 \\
0
\end{pmatrix}
\]

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Affine Transformations

- Loop transformations defined using affine mapping functions
  - Original iteration space $\Rightarrow$ Transformed iteration space
  - A one-dimensional affine transform ($\Phi$) for a statement $S$ is given by
    $$\Phi_S(x_S) = C_S \cdot \begin{pmatrix} x_S \\ n \\ 1 \end{pmatrix}$$
  - $\Phi$ represents a new loop in the transformed space
  - Set of linearly independent affine transforms
    - Define the transformed space
    - Define tiling hyperplanes for tiled code generation
Tiling

for (i=0; i<N; i++)
    x[i]=0;
for (j=0; j<N; j++)
    S: x[i] += a[j][i] * y[j];

for ( it =0; it<=floor(N-1,32);it++)
    for ( jt =0; jt<=floord(N-1,32);jt++)
    ...
    for ( i=max(32it ,0);
        i<=min(32it+31,N-1); i++)
    for ( j=max(32jt ,1);
        j<=min(32jt+31,N-1);j++)
    S: x[i] += a[j][i] * y[j];

\[
\begin{bmatrix}
    i \\
    j \\
    N \\
    1
\end{bmatrix} \geq 0
\]

\[
\begin{bmatrix}
    it \\
    jt \\
    i \\
    j \\
    N \\
    1
\end{bmatrix} \geq 0
\]

\[
\begin{bmatrix}
    T_s & 0 & iTs_s \\
    0 & D_s & T_s \\
    1 & 1
\end{bmatrix} \geq 0
\]

- Tiled iteration space
  - Higher-dimensional polytope
  - Supernode iterators
  - Intra-tile iterators

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PLUTO

- State-of-the-art polyhedral model based automatic parallelization system
- First approach to explicitly model tiling in a polyhedral transformation framework
- Finds a set of “good” affine transforms or tiling hyperplanes to address two key issues
  - effective extraction of coarse-grained parallelism
  - data locality optimization
- Handles sequences of imperfectly nested loops
- Uses state-of-the-art code generator CLooG
  - Takes original statement domains and affine transforms to generate transformed code
Affine Compiler Frameworks

Pros

- Powerful algebraic framework for abstracting dependences and transformations
- Enables the feasibility of automatic parallelization
  - Eases the burden of programmers

Cons

- Generated parallel code may have excessive barrier synchronization due to affine schedules
  - Loss of efficiency on multi-core systems due to load imbalance and poor scalability!
Aim and Approach

- Can we develop an automatic parallelization approach for asynchronous, load-balanced parallel execution?
- Utilize the powerful polyhedral model
  - To generate tiling hyperplanes (generate tiled code)
  - To derive inter-tile dependences
- Effectively schedule the tiles for parallel execution on the processor cores of a multi-core system
  - Dynamic (run-time) scheduling
Aim and Approach

- Each tile identified by affine framework is a “task” that is scheduled for execution
- Compile-time generation of following code segments
  - Code executed within a tile or task
  - Code to extract inter-tile (inter-task) dependences in the form of task dependence graph (TDG)
  - Code to dynamically schedule the tasks using critical path analysis on TDG to prioritize tasks
- Run-time execution of the compile-time generated code for efficient asynchronous parallelism

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System Overview

Pluto Optimization System

Task Dependence Graph Generator

Task Scheduler

Task Dependence Graph Generator

Inter-tile Dependence Extractor

TDG Code Generator

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Task Dependence Graph Generation

- Task Dependence Graph
  - DAG
    - Vertices – Tiles or tasks
    - Edges – Dependence between the corresponding tasks
  - Vertices and edges may be assigned weights
    - Vertex weight – based on task execution
    - Edge weight – based on communication between tasks
  - Current implementation
    - Unit weights for vertices and zero weights for edges

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Task Dependence Graph Generation

- Compile-time generation of TDG generation code
  - Code to enumerate the vertices
    - Scan the iteration space polytopes of all statements in the tiled domain, projected to contain only the supernode iterators
    - CLooG loop generator is used for scanning the polytopes
  - Code to create the edges
    - Requires extraction of inter-tile dependences
Inter-tile Dependence Abstraction
Inter-tile Dependence Abstraction

- Dependencies expressed in tiled domain using a higher-dimensional dependence polytope
- Project out intra-tile iterators from the system
- Resulting system characterizes inter-tile dependences
- Scan the system using CLooG to generate loop structure that has
  - Source tile iterators as outer loops
  - Target tile iterators as inner loops
- Loop structure gives code to generate edges in TDG

\[
\begin{align*}
\begin{pmatrix}
D_s & 0 \\
0 & D_t \\
-I & H
\end{pmatrix}
\begin{pmatrix}
i_s \\
1
\end{pmatrix}
\geq
\begin{pmatrix}
0 \\
0
\end{pmatrix}
= \begin{pmatrix}
0 \\
0
\end{pmatrix}
\end{align*}
\]

\[
\begin{align*}
\begin{pmatrix}
T_s & 0 & 0 & 0 \\
0 & D_s & 0 & 0 \\
0 & 0 & T_t & 0 \\
0 & 0 & 0 & D_t \\
0 & -I & 0 & H
\end{pmatrix}
\begin{pmatrix}
i't_s \\
i't_t \\
1
\end{pmatrix}
\geq
\begin{pmatrix}
0 \\
0
\end{pmatrix}
= \begin{pmatrix}
0 \\
0
\end{pmatrix}
\end{align*}
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i't'_t \\
1
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\geq
\begin{pmatrix}
0 \\
0
\end{pmatrix}
\end{align*}
\]
### Static Affine Scheduling

A diagram illustrating the process of scheduling tasks in a parallel environment, specifically focusing on static affine scheduling. The diagram shows a grid representing time and core allocation, with tasks assigned to specific time slots and cores. The vertical axis denotes time, and the grid is partitioned into time slots labeled $t(0,0)$ to $t(4,4)$.

Core allocation is denoted using the labels $C1$ and $C2$. The schedule is represented with tasks assigned to specific grid cells, indicating how tasks are distributed across time and cores.

The diagram also includes a legend for the affine schedule, showing how tasks are mapped to specific time slots and cores. This visual representation helps in understanding the dynamic scheduling process and how tasks are effectively parallelized across multiple cores for optimal performance.

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**Legend for Schedule**

- $t(0,0)$ to $t(4,4)$ represent time slots.
- $C1$ and $C2$ denote core allocation.
- The schedule assigns tasks to specific time and core combinations.
Scheduling strategy: critical path analysis for prioritizing tasks in TDG

Priority metrics associated with vertices

- $topL(v)$ - length of the longest path from the source vertex (i.e., the vertex with no predecessors) in $G$ to $v$, excluding the vertex weight of $v$
- $bottomL(v)$ - length of the longest path from $v$ to the sink (vertex with no children), including the vertex weight of $v$

Tasks are prioritized based on

- sum of their top and bottom levels or
- just the bottom level
Tasks are scheduled for execution based on
- completion of predecessor tasks
- $bottomL(v)$ priority
- availability of processor core
Affine vs. Dynamic Scheduling

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Run-time Execution

1: Execute TDG generation code to create a DAG G
2: Calculate $topL(v)$ and $bottomL(v)$ for each vertex $v$ in $G$, to prioritize the vertices
3: Create a Priority Queue $PQ$
4: $PQ.insert(\text{ vertices with no parents in } G)$
5: while not all vertices in $G$ are processed do
6: \hspace{1em} $taskid = PQ.extract(\ )$
7: \hspace{1em} Execute $taskid$ // Compute code
8: \hspace{1em} Remove all outgoing edges of $taskid$ from $G$
9: \hspace{1em} $PQ.insert(\text{ vertices with no parents in } G)$
10: end while
Experiments

 Experimental Setup

- a quad-core Intel Core 2 Quad Q6600 CPU
  - clocked at 2.4 GHz (1066 MHz FSB)
  - 8MB L2 cache (4MB shared per core pair)
  - Linux kernel version 2.6.22 (x86-64)
- a dual quad core Intel Xeon(R) E5345 CPU
  - clocked at 2.33 GHz
  - each chip having a 8MB L2 cache (4MB shared per core pair)
  - Linux kernel version 2.6.18
- ICC 10.x compiler
  - Options: -fast -funroll-loops (-openmp for parallelized code)
Experiments

Performance of LU on Quad Core

Performance of LU on Dual Quad Core
Experiments
Experiments

Performance of Cholesky on Quad Core

Performance of Cholesky on Dual Quad Core

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Discussion

- Absolute achieved GFLOPs performance is currently lower than the machine peak by over a factor of 2
- Single-node performance sub-optimal
  - No pre-optimized tuned kernels
    - E.g. BLAS kernels like DGEMM in LU code
- Work in progress to provide
  - Identification of tiles where pre-optimized kernels can be substituted
Related Work

- Dongarra et al. - PLASMA (Parallel Linear Algebra for Scalable Multi-core Architectures)
  - LAPACK codes optimization
    - Manual rewriting of LAPACK routines
    - Run-time scheduling framework
- Robert van de Geijn et al. - FLAME
- Dynamic run-time parallelization [LRPD, Mitosis, etc.]
  - Basic difference: Dynamic scheduling of loop computations amenable to compile-time characterization of dependences
- Plethora of work on DAG scheduling
Summary

- Developed a fully-automatic approach for asynchronous load balanced parallel execution on multi-core systems

Basic idea
- To automatically generate tiled code along with additional helper code at compile time
- Role of helper code at run time
  - to dynamically extract inter-tile data dependences
  - to dynamically schedule the tiles on the processor cores

- Achieved significant improvement over programs automatically parallelized using affine compiler frameworks
Thank You