CIS 775: Computer Architecture
Spring 2001

Course Web Page: http://www.cis.ohio-state.edu/ srini/775/

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Grader: TBA
Office:
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Office Hours: TBA

Class Hours: MWF 8:30-9:20pm

Prerequisites: CIS 675 and CIS 660

Syllabus: Fundamentals of Computer Design, Performance Measures, Instruction set Design, Reduced Instruction Set Architecture (RISC), Introduction to Pipelining, Advanced Pipelining Techniques, Memory Hierarchy and Cache Design, Storage Systems, Introduction to Vector and Parallel Computer Architectures.

Objectives:

1. To understand and appreciate the principles and tradeoffs (cost/performance, speed/flexibility) behind the design of modern computer systems in a qualitative and quantitative fashion.
2. To understand issues in choosing and designing an instruction set.
3. To learn the concepts of basic pipelining and advanced pipelining techniques.
4. To learn issues related to hierarchical memory system design.
5. To obtain an overview of vector and parallel computer architectures.

Text Book: Computer Architecture A Quantitative Approach by John Hennessy and David Patterson, Morgan Kauffman, 1996 (second edition).

Grading:

Homeworks:	20 %
Simulation Labs:	20 %
Midterm:	25 %
Final:	35 %

Homeworks: There will be four or five problem sets. The problem sets will be distributed before one week of the due date. Late homeworks will not be accepted. An exception to this rule requires that you have a strong and convincing reason. *If you have such a reason, you will have to let me know about it in advance.*

Labs using Simulators: There will be two or three labs involving simulation experiments. The labs will involve using DLX simulator *dlxsim* to evaluate instruction statistics, pipelining techniques and branch mechanisms. The first lab will expose you to the *dlxsim* simulator. The *Dinero* simulator will be used in the second/third lab to evaluate different cache organizations. The labs will be distributed around 10 days in advance. Both the simulators run on the CIS SUN Solaris systems. The labs need to be done individually. Each student has been assigned an account in the CIS system to carry out these simulation. If you do not have an account please let me know about it.

If you are interested in getting familiarized with these simulator environments earlier, you can refer to the respective man pages in `/usr/class/cis775/man` directory. Manual pages for DLX simulator are available in both postscript (file `dlxsim.ps`) and PDF (file `dlxsim.pdf`) format. You can view the postscript file using 'ghostview' command and the PDF file using 'acroread' command. Similarly, the man page for *Dinero* is available as an ascii *dinero.cat* file in this directory. The corresponding programs (*dlxcc* for generating assembly code from a C program, *dlxsim* for executing the assembly program on DLX processor, and *dinero* to study the impact of cache organizations) can be invoked from `/usr/class/cis775/solaris/bin` directory. (This binary version works on SUN solaris platform, the standard UNIX environment used in the CIS environment.) Detailed guidelines to carry out these labs will be provided with the homeworks and lab handouts.

Examinations: There will be two examinations. A midterm will be held on the 15th class of the quarter and a final at the end of the quarter, as indicated below. Examinations are likely to be **closed** book, and **closed** notes, and are most definitely **closed** neighbors.

MIDTERM	Tentative	April 27	8:30-10:00am	in class
FINAL	(Regular)	June 4	7:30-9:18am	in class
FINAL	(Graduating Seniors)	May 29	2:30pm-4:30pm	TBD

Electronic Distribution of Class Materials: During the first week of the class, I will collect e-mail addresses of all students to create an electronic mailing list. Make sure that you give me your e-mail address (campus or work) on the system you frequently log on. If you do not receive any e-mail from me by the second week of the class, please check with me to ensure that your name is in the mailing list. I will use this mailing list throughout the quarter to make important announcements and clarifications about homework problems, if needed.

All homeworks will be made available (PDF versions) through the Web. The URL is `http://www.cis.ohio-state.edu/~srini/775`. An announcement will be made in class when each homework is placed on the Web.

Tentative[1] Class Schedule

# Weeks	Topics	Readings from T
0.33	Introduction; Course Overview	
	Technology Trends	1.1–1.3
	Cost and Performance	1.4–1.5
1.0	Quantitative Principles of Computer Design	1.6
	Reading Assignment	1.7–1.9
	Classifying Instruction Set Architectures	2.1–2.2
	Features of Instruction Set	2.3–2.6
0.67	DLX Architecture	2.8
	Reading Assignment	2.7,2.9–2.10
1.0	Basic Pipelining and Hazards	3.1–3.3
1.0	Data Hazards	3.4
	Control Hazards	3.5
1.0	Interrupts and Exceptions	3.6
	Multicycle Operations	3.7
	Crosscutting Issues in Pipelining	3.8
	Reading Assignment	3.9–3.10
1.0	Instructional-Level Parallelism	4.1
	MIDTERM	
	Dynamic Scheduling	4.2
1.0	Dynamic Scheduling (Contd.)	4.2
	Memory-Hierarchy Design and Caches	5.1–5.2
	Reducing Cache Misses	5.3
1.0	Reducing Cache Miss Penalty and Hit Time	5.4–5.5
	Main Memory Design Issues	5.6
	Crosscutting Issues	5.9
	Reading Assignment	5.10
1.0	Vector Processors	B.1–B.3
1.0	Vector Processor Performance	B.4–B.5
	Overview of Interconnection Networks	7.1–7.5
	Overview of Multiprocessors	8.1–8.4
	Course Review	

[1] Subject to change depending on class progress.