1. (20 points) Consider a memory subsystem with a capacity of $2^{32}$ bytes. This has a 4K byte cache with 4-double-word (each double-word being 8 bytes) block size.

For the following four cache organizations, determine how many bits are used for tag, index, and block offset, respectively.

(a) direct-mapped
(b) 2-way set-associative
(c) 8-way set-associative
(d) fully set-associativity

2. Consider a 32-double-word direct-mapped and write-through data cache with 1-double-word block size. The following loop has been translated to the corresponding MIPS program. Each element of the array A is a double-word. The array is stored in the memory starting from address 0x1000 (Hex).

```
for i:=0 to 127 do
```

(a) (20 points) Considering only data cache, determine the percentage of read-hit, read-miss, write-hit, and write-miss for data references in the above program. Explain your answers.

(b) (10x3=30 points) Consider the following variations to the data cache organization while keeping the cache capacity the same (i.e., 32 double-word)

i. block-size of 2 double-word, direct-mapped and write-through
ii. block-size of 4 double-word, 2-way set-associative and write-through
iii. block-size of 4 double-word, fully-associative and write-back

How do the percentages of read-hit, read-miss, write-hit and write-miss for data references change for the above program with these cache organizations? Explain your answers.

3. (30 points) Consider a 4-way interleaved main memory organization. The width of each memory bank is double-word. Assume multiplexed address and data lines (i.e. putting an address and reading/writing data can not be overlapped). Consider the following timings: 2 clock cycle to put the address, 8 clock cycles to access the interleaved memory and 2 clock cycles to transfer each double-word.

Determine the memory penalty the program indicated in Problem #2 will have for the four cache organizations (indicated in Problem #2). Explain your answers.