## Tentative Class Schedule

<table>
<thead>
<tr>
<th>Week</th>
<th>Topics</th>
<th>Readings from Text</th>
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</table>
| Sept 22 | Introduction; Course Overview  
Technology Trends            | 1.1–1.3            |
| Sept 27 | Cost, Performance & Dependability  
Quantitative Principles of Computer Design  
Reading Assignment  
Classifying Instruction Set Architectures and Features | 1.4–1.8  
1.9  
1.10–1.11  
B.1–B.7 |
| Oct 4  | Role of Compilers and MIPS Architecture  
Basic Pipelining  
Hw#1 due (Oct 6) | B.8–B.9  
A.1 |
| Oct 11 | Data and Control Hazards  
Pipelining Implementations and Multicycle operations | A.2  
A.3–A.4 |
| Oct 18 | Multicycle operations  
Hw#2 due (Oct 18) | A.5 |
| Oct 25 | MIPS R4000 pipeline  
Crosscutting Issues in Pipelining  
MIDTERM (Oct 27) | A.6  
A.7 |
| Nov 1  | Instructional-Level Parallelism  
Dynamic Scheduling and Branch Prediction  
Lab#1 due (Nov 3) | 2.1–2.2  
2.3–2.5  
Lab#1 due (Nov 3) |
| Nov 8  | Hardware-based Speculation  
Advanced Techniques | 2.6–2.7  
2.8–2.10 |
| Nov 15 | Memory-Hierarchy Design and Caches  
Cache Optimizations  
Hw#3 due (Nov 15) | C.1, C.2 and 5.1  
C.3 and 5.2  
Hw#3 due (Nov 15) |
| Nov 22 | Virtual Memory  
Main Memory Design Issues  
Lab#2 due (Nov 22) | C.4  
5.3 |
| Nov 29 | Overview of Interconnection Networks  
Overview of Multiprocessing  
Overview of Latest Multicore Processors  
Hw#4 due (Dec 1)  
FINAL Exam (Dec 6) | Appendix E  
4.1  
Lab#2 due (Nov 22)  
Hw#4 due (Dec 1)  
FINAL Exam (Dec 6) |