NVIDIA CUDA
Compute Unified Device Architecture

Programming Guide

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1.1 The Graphics Processor Unit as a Data-Parallel Computing Device

In a matter of just a few years, the programmable graphics processor unit has evolved into an absolute computing workhorse, as illustrated by Figure 1-1. With multiple cores driven by very high memory bandwidth, today's GPUs offer incredible resources for both graphics and non-graphics processing.

![Figure 1-1. Floating-Point Operations per Second for the CPU and GPU](image)

The main reason behind such an evolution is that the GPU is specialized for compute-intensive, highly parallel computation – exactly what graphics rendering is about – and therefore is designed such that more transistors are devoted to data processing rather than data caching and flow control, as schematically illustrated by Figure 1-2.
Figure 1-2. The GPU Devotes More Transistors to Data Processing

More specifically, the GPU is especially well-suited to address problems that can be expressed as data-parallel computations – the same program is executed on many data elements in parallel – with high arithmetic intensity – the ratio of arithmetic operations to memory operations. Because the same program is executed for each data element, there is a lower requirement for sophisticated flow control; and because it is executed on many data elements and has high arithmetic intensity, the memory access latency can be hidden with calculations instead of big data caches.

Data-parallel processing maps data elements to parallel processing threads. Many applications that process large data sets such as arrays can use a data-parallel programming model to speed up the computations. In 3D rendering large sets of pixels and vertices are mapped to parallel threads. Similarly, image and media processing applications such as post-processing of rendered images, video encoding and decoding, image scaling, stereo vision, and pattern recognition can map image blocks and pixels to parallel processing threads. In fact, many algorithms outside the field of image rendering and processing are accelerated by data-parallel processing, from general signal processing or physics simulation to computational finance or computational biology.

Up until now, however, accessing all that computation power packed into the GPU and efficiently leveraging it for non-graphics applications remained tricky:

- The GPU could only be programmed through a graphics API, imposing a high learning curve to the novice and the overhead of an inadequate API to the non-graphics application.
- The GPU DRAM could be read in a general way – GPU programs can *gather* data elements from any part of DRAM – but could not be written in a general way GPU programs cannot *scatter* information to any part of DRAM, removing a lot of the programming flexibility readily available on the CPU.
- Some applications were bottlenecked by the DRAM memory bandwidth, under-utilizing the GPU's computation power.

This document describes a novel hardware and programming model that is a direct answer to these problems and exposes the GPU as a truly generic data-parallel computing device.
1.2 CUDA: A New Architecture for Computing on the GPU

CUDA stands for Compute Unified Device Architecture and is a new hardware and software architecture for issuing and managing computations on the GPU as a data-parallel computing device without the need of mapping them to a graphics API. It is available for the GeForce 8800 Series and beyond. The operating system’s multitasking mechanism is responsible for managing the access to the GPU by several CUDA and graphics applications running concurrently.

The CUDA software stack is composed of several layers as illustrated in Figure 1-3: a hardware driver, an application programming interface (API) and its runtime, and two higher-level mathematical libraries of common usage, CUFFT and CUBLAS that are both described in separate documents (cufft_library.pdf and cublas_library.pdf). The hardware has been designed to support lightweight driver and runtime layers, resulting in high performance.

Figure 1-3. Compute Unified Device Architecture Software Stack

The CUDA API comprises an extension to the C programming language for a minimum learning curve (see Chapter 4).
CUDA provides general DRAM memory addressing as illustrated in Figure 1-4 for more programming flexibility: both scatter and gather memory operations. From a programming perspective, this translates into the ability to read and write data at any location in DRAM, just like on a CPU.

Figure 1-4. The Gather and Scatter Memory Operations
CUDA features a parallel data cache or on-chip shared memory with very fast general read and write access, that threads use to share data with each other (see Chapter 3). As illustrated in Figure 1-5, applications can take advantage of it by minimizing overfetch and round-trips to DRAM and therefore becoming less dependent on DRAM memory bandwidth.

Figure 1-5. Shared Memory Brings Data Closer to the ALUs
1.3 Document’s Structure

This document is organized into the following chapters:

- Chapter 1 contains a general introduction to CUDA.
- Chapter 2 outlines the programming model.
- Chapter 3 describes its hardware implementation.
- Chapter 4 describes the CUDA API and runtime.
- Chapter 5 gives the technical specifications of GeForce 8800 Series.
- Chapter 6 gives some guidance on how to achieve maximum performance.
- Chapter 7 illustrates the previous chapters by walking through the code of some simple example.
2.1 A Highly Multithreaded Coprocessor

When programmed through CUDA, the GPU is viewed as a compute device capable of executing a very high number of threads in parallel. It operates as a coprocessor to the main CPU, or host. In other words, data-parallel, compute-intensive portions of applications running on the host are off-loaded onto the device.

More precisely, a portion of an application that is executed many times, but independently on different data, can be isolated into a function that is executed on the device as many different threads. To that effect, such a function is compiled to the instruction set of the device and the resulting program, called a kernel, is downloaded to the device.

Both the host and the device maintain their own DRAM, referred to as host memory and device memory, respectively. One can copy data from one DRAM to the other through optimized API calls that utilize the device’s high-performance Direct Memory Access (DMA) engines.

2.2 Thread Batching

The batch of threads that executes a kernel is organized as a grid of thread blocks as described in Sections 2.2.1 and 2.2.2 and illustrated in Figure 2-1.

2.2.1 Thread Block

A thread block is a batch of threads that can cooperate together by efficiently sharing data through some fast shared memory and synchronizing their execution to coordinate memory accesses. More precisely, one can specify synchronization points in the kernel, where threads in a block are suspended until they all reach the synchronization point.

Each thread is identified by its thread ID, which is the thread number within the block. To help with complex addressing based on the thread ID, an application can also specify a block as a two- or three-dimensional array of arbitrary size and identify each thread using a 2- or 3-component index instead. For a two-
dimensional block of size $(D_x, D_y)$, the thread ID of a thread of index $(x, y)$ is $(x + y \times D_x)$ and for a three-dimensional block of size $(D_x, D_y, D_z)$, the thread ID of a thread of index $(x, y, z)$ is $(x + y \times D_x + z \times D_x \times D_y)$.

2.2.2 Grid of Thread Blocks

There is a limited maximum number of threads that a block can contain. However, blocks that execute the same kernel can be batched together into a grid of blocks, so that the total number of threads that can be launched in a single kernel invocation is much larger. This comes at the expense of reduced thread cooperation, because threads in different thread blocks from the same grid cannot communicate and synchronize with each other. This model allows kernels to efficiently run without recompilation on various devices with different parallel capabilities: A device may run all the blocks of a grid sequentially if it has very few parallel capabilities, or in parallel if it has a lot of parallel capabilities, or usually a combination of both.

Each block is identified by its block ID, which is the block number within the grid. To help with complex addressing based on the block ID, an application can also specify a grid as a two-dimensional array of arbitrary size and identify each block using a 2-component index instead. For a two-dimensional block of size $(D_x, D_y)$, the block ID of a block of index $(x, y)$ is $(x + y \times D_x)$. 
The host issues a succession of kernel invocations to the device. Each kernel is executed as a batch of threads organized as a grid of thread blocks.

Figure 2-1. Thread Batching
2.3 Memory Model

A thread that executes on the device has only access to the device’s DRAM and on-chip memory through the following memory spaces, as illustrated in Figure 2-2:

- Read-write per-thread registers,
- Read-write per-thread local memory,
- Read-write per-block shared memory,
- Read-write per-grid global memory,
- Read-only per-grid constant memory,
- Read-only per-grid texture memory.

The global, constant, and texture memory spaces can be read from or written to by the host and are persistent across kernel calls by the same application.

The global, constant, and texture memory spaces are optimized for different memory usages (see Sections 6.1.2.1, 6.1.2.2, and 6.1.2.3). Texture memory also offers different addressing modes, as well as data filtering, for some specific data formats (see Section 4.3.4).
A thread has access to the device's DRAM and on-chip memory through a set of memory spaces of various scopes.

Figure 2-2. Memory Model
Chapter 3.
Hardware Implementation

3.1 A Set of SIMD Multiprocessors with On-Chip Shared Memory

The device is implemented as a set of multiprocessors as illustrated in Figure 3-1. Each multiprocessor has a Single Instruction, Multiple Data architecture (SIMD): At any given clock cycle, each processor of the multiprocessor executes the same instruction, but operates on different data.

Each multiprocessor has on-chip memory of the four following types:

- One set of local 32-bit registers per processor,
- A parallel data cache or shared memory that is shared by all the processors and implements the shared memory space,
- A read-only constant cache that is shared by all the processors and speeds up reads from the constant memory space, which is implemented as a read-only region of device memory,
- A read-only texture cache that is shared by all the processors and speeds up reads from the texture memory space, which is implemented as a read-only region of device memory.

The local and global memory spaces are implemented as read-write regions of device memory and are not cached.

Each multiprocessor accesses the texture cache via a texture unit that implements the various addressing modes and data filtering mentioned in Section 2.3.
A set of SIMD multiprocessors with on-chip shared memory.

Figure 3-1. Hardware Model

3.2 Execution Model

A grid of thread blocks is executed on the device by executing one or more blocks on each multiprocessor using time slicing: Each block is split into SIMD groups of threads called warps; each of these warps contains the same number of threads, called the warp size, and is executed by the multiprocessor in a SIMD fashion; a thread scheduler periodically switches from one warp to another to maximize the use of the multiprocessor’s computational resources.
The way a block is split into warps is always the same; each warp contains threads of consecutive, increasing thread indices with the first warp containing thread 0.

A block is processed by only one multiprocessor, so that the shared memory space resides in the on-chip shared memory leading to very fast memory accesses.

A multiprocessor can process several blocks concurrently by partitioning among them the sets of registers and the shared memory. More precisely, the number of registers available per thread is equal to the total number of registers per multiprocessor divided by the number of concurrent threads rounded up to the nearest multiple of 64, where the number of concurrent threads is equal to the number of concurrent blocks multiplied by the number of threads per block.

The issue order of the warps within a block is undefined, but their execution can be synchronized, as mentioned in Section 2.2.1, to coordinate global or shared memory accesses. If the instruction executed by the threads of a warp writes to the same location in global or shared memory, the order of the writes is undefined.

The issue order of the blocks within a grid of thread blocks is undefined and there is no synchronization mechanism between blocks, so threads from two different blocks of the same grid cannot safely communicate with each other through global memory.
Chapter 4. Application Programming Interface

4.1 An Extension to the C Programming Language

The goal of the CUDA programming interface is to provide a relatively simple path for users familiar with the C programming language to easily write programs for execution by the device.

It consists of:

- A minimal set of extensions to the C language, described in Section 4.2, that allow the programmer to target portions of the source code for execution on the device;
- A runtime library split into:
  - A host component, described in Section 4.5, that runs on the host and provides functions to control and access one or more compute devices from the host;
  - A device component, described in Section 4.4, that runs on the device and provides device-specific functions;
  - A common component, described in Section 4.3, that provides built-in vector types and a subset of the C standard library that are supported in both host and device code.

It should be emphasized that the only functions from the C standard library that are supported to run on the device are the functions provided by the common runtime component.

4.2 Language Extensions

The extensions to the C programming language are four-fold:

- Function type qualifiers to specify whether a function executes on the host or on the device and whether it is callable from the host or from the device (Section 4.2.1);
- Variable type qualifiers to specify the memory location on the device of a variable (Section 4.2.2);
A new directive to specify how a kernel is executed on the device from the host (Section 4.2.3);

Four built-in variables that specify the grid and block dimensions and the block and thread indices (Section 4.2.4).

These extensions come with some restrictions described in each of the sections below. `nvcc` will give an error or a warning on some violations of these restrictions, but some of them cannot be detected.

Each source file containing CUDA language extensions must be compiled with the CUDA compiler `nvcc`, as briefly described in Section 4.2.5. A detailed description of `nvcc` can be found in a separate document `nvcc.pdf`.

### 4.2.1 Function Type Qualifiers

#### 4.2.1.1 __device__

The __device__ qualifier declares a function that is:

- Executed on the device
- Callable from the device only.

#### 4.2.1.2 __global__

The __global__ qualifier declares a function as being a kernel. Such a function is:

- Executed on the device,
- Callable from the host only.

#### 4.2.1.3 __host__

The __host__ qualifier declares a function that is:

- Executed on the host,
- Callable from the host only.

It is equivalent to declare a function with only the __host__ qualifier or to declare it without any of the __host__, __device__, or __global__ qualifier; in either case the function is compiled for the host only.

However, the __host__ qualifier can also be used in combination with the __device__ qualifier, in which case the function is compiled for both the host and the device.

#### 4.2.1.4 Restrictions

__device__ and __global__ functions do not support recursion.

__device__ and __global__ functions cannot declare static variables inside their body.

__device__ and __global__ functions cannot have a variable number of arguments.

__device__ functions cannot have their address taken; function pointers to __global__ functions, on the other hand, are supported.

The __global__ and __host__ qualifiers cannot be used together.
__global__ functions must have void return type.

Any call to a __global__ function must specify its execution configuration as described in Section 4.2.3.

A call to a __global__ function is synchronous, meaning it blocks until completion.

__global__ function parameters are currently passed via shared memory to the device and limited to 256 bytes.

4.2.2 Variable Type Qualifiers

4.2.2.1 __device__

The __device__ qualifier declares a variable that resides on the device.

At most one of the other type qualifiers defined in the next three sections may be used together with __device__ to further specify which memory space the variable belongs to. If none of them is present, the variable:

- Resides in global memory space,
- Has the lifetime of an application,
- Is accessible from all the threads within the grid and from the host through the runtime library.

4.2.2.2 __constant__

The __constant__ qualifier, optionally used together with __device__, declares a variable that:

- Resides in constant memory space,
- Has the lifetime of an application,
- Is accessible from all the threads within the grid and from the host through the runtime library.

4.2.2.3 __shared__

The __shared__ qualifier, optionally used together with __device__, declares a variable that:

- Resides in the shared memory space of a thread block,
- Has the lifetime of the block,
- Is only accessible from all the threads within the block.

When declaring a variable in shared memory as an external array such as

```
extern __shared__ float shared[];
```

the size of the array is determined at launch time (see Section 4.2.3). All variables declared in this fashion, start at the same address in memory, so that the layout of the variables in the array must be explicitly managed through offsets. For example, if one wants the equivalent of

```
short array0[128];
float array1[64];
int array2[256];
```
in dynamically allocated shared memory, one could define the arrays the following way

```c
extern __shared__ short array0[]; const int size0 = 128;
extern __shared__ float array1[]; const int size1 = 64;
extern __shared__ int   array2[]; const int size2 = 256;
```

and index into them using the following macros

```c
#define ARRAY0(i) (array0[i])
#define ARRAY1(i) 
  (array1[(i)+((size0+1)*sizeof(array0[0]))/sizeof(array1[0])])
#define ARRAY2(i) 
  (array2[(i)+((size1+1)*sizeof(array1[0]))/sizeof(array2[0])])
```

### 4.2.2.4 Restrictions

These qualifiers are not allowed on `struct` and `union` members, on formal parameters and on local variables within a function that executes on the host.

- `__shared__` and `__constant__` cannot be used in combination with each other.
- `__shared__` and `__constant__` variables have implied static storage.
- `__constant__` variables cannot be assigned to from the device, only from the host. They are therefore only allowed at file scope.
- `__shared__` variables cannot have an initialization as part of their declaration.

An automatic variable declared in device code without any of these qualifiers generally resides in a register. However in some cases the compiler might choose to place it in local memory. This is often the case for large structures or arrays that would consume too much register space, and arrays for which the compiler cannot determine that they are indexed with constant quantities. Inspection of the `.ptx` assembly code (obtained by compiling with the `-ptx` or `-keep` option) will tell if a variable has been placed in local memory during the first compilation phases as it will be declared using the `.local` mnemonic and accessed using the `ld.local` and `st.local` mnemonics. If it has not, subsequent compilation phases might still decide otherwise though if they find it consumes too much register space for the targeted architecture.

Pointers in code that is executed on the device are restricted to only point to memory allocated or declared in the global memory space. Such pointers are either passed as arguments to any `__global__` or `__device__` function, or obtained as the result of taking the address of a variable residing in the global memory space.

Dereferencing a pointer either to global memory in code that is executed on the host or to host memory in code that is executed on the device results in an undefined behavior, most often in a segmentation fault and application termination.

### 4.2.3 Execution Configuration

Any call to a `__global__` function must specify the execution configuration for that call.

The execution configuration defines the dimension of the grid and blocks that will be used to execute the function on the device. It is specified by inserting an
expression of the form $<<< \text{Dg, Db, Ns} >>>$ between the function name and the parenthesized argument list, where:

- Dg is of type \text{dim3} (see Section 4.3.1.2) and specifies the dimension and size of the grid, such that $\text{Dg.x \times Dg.y}$ equals the number of blocks being launched;
- Db is of type \text{dim3} (see Section 4.3.1.2) and specifies the dimension and size of each block, such that $\text{Db.x \times Db.y \times Db.z}$ equals the number of threads per block;
- Ns is of type \text{size_t} and specifies the number of bytes in shared memory that is dynamically allocated for this call in addition to the statically allocated memory; this dynamically allocated memory is used by any of the variables declared as an external array as mentioned in Section 4.2.2.3; Ns is an optional argument which defaults to 0.

The arguments to the execution configuration are evaluated before the actual function arguments.

As an example, a function declared as

```c
__global__ void Func(float* parameter);
```

must be called like this:

```c
Func<<< Dg, Db, Ns >>>(parameter);
```

### 4.2.4 Built-in Variables

#### 4.2.4.1 gridDim
This variable is of type \text{dim3} (see Section 4.3.1.2) and contains the dimensions of the grid.

#### 4.2.4.2 blockIdx
This variable is of type \text{uint3} (see Section 4.3.1.1) and contains the block index within the grid.

#### 4.2.4.3 blockDim
This variable is of type \text{dim3} (see Section 4.3.1.2) and contains the dimensions of the block.

#### 4.2.4.4 threadIdx
This variable is of type \text{uint3} (see Section 4.3.1.1) and contains the thread index within the block.

#### 4.2.4.5 Restrictions
- It is not allowed to take the address of any of the built-in variables.
- It is not allowed to assign values to any of the built-in variables.

### 4.2.5 Compilation with NVCC

\text{nvcc} is a compiler driver that simplifies the process of compiling CUDA code: It provides simple and familiar command line options and executes them by invoking the collection of tools that implement the different compilation stages.
Chapter 4. Application Programming Interface

nvcc’s basic workflow consists in separating device code from host code and compiling the device code into a binary form or cubin object. The generated host code is output either as C code that is left to be compiled using another tool or as object code directly by invoking the host compiler during the last compilation stage.

Applications can either ignore the generated host code and load the cubin object onto the device and launch the device code using the CUDA driver API (see Section 4.5.3), or link to the generated host code, which includes the cubin object as a global initialized data array and contains a translation of the execution configuration syntax described in Section 4.2.3 into the necessary CUDA runtime startup code to load and launch each compiled kernel (see Section 4.5.2).

A detailed description of nvcc can be found in a separate document nvcc.pdf.

4.3 Common Runtime Component

The common runtime component can be used by both host and device functions.

4.3.1 Built-in Vector Types

4.3.1.1 char1, uchar1, char2, uchar2, char3, uchar3, char4, uchar4, short1, ushort1, short2, ushort2, short3, ushort3, short4, ushort4, int1, uint1, int2, uint2, int3, uint3, int4, uint4, long1, ulong1, long2, ulong2, long3, ulong3, long4, ulong4, float1, float2, float3, float4

These are vector types derived from the basic integer and floating-point types. They are structures and the 1st, 2nd, 3rd, and 4th components are accessible through the fields x, y, z, and w, respectively. They all come with a constructor function of the form make_<type name>; for example,

\[ \text{int2 make_int2(int x, int y);} \]

which creates a vector of type int2 with value \((x, y)\).

4.3.1.2 dim3

This type is an integer vector type based on uint3 that is used to specify dimensions. When defining a variable of type dim3, any component left unspecified is initialized to 1.

4.3.2 Mathematical Functions

Table A-1 in Appendix A contains a comprehensive list of the C/C++ standard library mathematical functions that are currently supported, along with their respective error bounds when executed on the device.

When executed on the host, a given function uses the C runtime implementation if available.
4.3.3 Time Function

\texttt{clock_t clock();}

returns the value of a counter that is incremented every clock cycle. Sampling this counter at the beginning and at the end of a kernel, taking the difference of the two samples, and recording the result per thread provides a measure for each thread of the number of clock cycles taken by the device to completely execute the thread, but not of the number of clock cycles the device actually spent executing thread instructions. The former number is greater that the latter since threads are time sliced.

4.3.4 Texture Type

Texture memory is exclusively accessed through \textit{texture references}. A texture reference is bound to some region of memory, called \textit{texture}, and defines a specific access mode for this texture. In particular, a texture reference has a dimensionality that specifies whether the texture it is bound to is addressed either as a one-dimensional array using one texture coordinate, or as a two-dimensional array using two texture coordinates. Elements of the array are called \textit{texels} and the process of reading data from a texture via a texture reference using some input texture coordinates is called \textit{texture fetching}.

A texture reference is declared at file scope as a variable of type \texttt{texture}:

\texttt{texture<Type, Dim, ReadMode> texRef;}

where:

- \textbf{Type} specifies the type of data that is returned when fetching the texture; \textbf{Type} is restricted to the basic integer and floating-point types and any of the vector types defined in Section 4.3.1.1;
- \textbf{Dim} specifies the dimensionality of the texture reference and is equal to 1 or 2; \textbf{Dim} is an optional argument which defaults to 1;
- \textbf{ReadMode} is equal to \texttt{cudaReadModeNormalizedFloat} or \texttt{cudaReadModeElementType}; if it is \texttt{cudaReadModeNormalizedFloat} and \textbf{Type} is an integer type, the value is actually returned as floating-point type and the full range of the integer type is mapped to \([0, 1]\); for example, an unsigned 8-bit texture element with the value 0xff reads as 1; if it is \texttt{cudaReadModeElementType}, no conversion is performed; \textbf{ReadMode} is an optional argument which defaults to \texttt{cudaReadModeElementType}.

The \texttt{texture} type is a structure with the following fields:

- \textbf{channelDesc} which describes the format of the value that is returned when fetching the texture; \textbf{channelDesc} is of the following type:

\begin{verbatim}
struct cudaChannelFormatDesc {
    int x, y, z, w;
    enum cudaChannelFormatKind f;
};
\end{verbatim}

where \textbf{\(x, y, z, \) and \(w\)} are equal to the number of bits of each component of the returned value and \textbf{\(f\)} is:

- \texttt{cudaChannelFormatKindSigned} if these components are of signed integer type,
CUDA Channel Format Kind

- `cudaChannelFormatKindUnsigned` if they are of unsigned integer type,
- `cudaChannelFormatKindFloat` if they are of floating point type;

- `normalized` which specifies whether texture coordinates are normalized or not; if it is non-zero, all elements in the texture are addressed with texture coordinates in the range \([0, 1]\) rather than in the range \([0, width-1]\) or \([0, height-1]\), where `width` and `height` are the texture sizes;

- `addressMode` which specifies the addressing mode, that is how out-of-range texture coordinates are handled; `addressMode` is an array of size two whose first and second elements specify the addressing mode for the first and second texture coordinates, respectively; the addressing mode is equal to either `cudaAddressModeClamp`, in which case out-of-range texture coordinates are clamped to the valid range, or `cudaAddressModeWrap`, in which case out-of-range texture coordinates are wrapped to the valid range;

- `filterMode` which specifies the filtering mode, that is how the value returned when fetching the texture is computed based on the input texture coordinates; `filterMode` is equal to `cudaFilterModePoint` or `cudaFilterModeLinear`; if it is `cudaFilterModePoint`, the returned value is the texel whose texture coordinates are the closest to the input texture coordinates; if it is `cudaFilterModeLinear`, the returned value is the linear interpolation of the two (for a one-dimensional texture) or four (for a two-dimensional texture) texels whose texture coordinates are the closest to the input texture coordinates; `cudaFilterModeLinear` is only valid for returned values of floating-point type.

All these fields, but `channelDesc`, may be directly modified in host code.

A texture is allocated either in linear memory or as an array (see Section 4.5.1.2). Textures allocated in linear memory can only be addressed using non-normalized integer texture coordinates and do not support the linear filtering mode.

## 4.4 Device Runtime Component

The device runtime component can only be used in device functions.

### 4.4.1 Mathematical Functions

For some of the functions of Table A-1, a less accurate, but faster version exists in the device runtime component; it has the same name prefixed with `__` (such as `__sin(x)`). These functions are listed in Table A-2, along with their respective error bounds.

The compiler has an option `-use_fast_math` to force every function to compile to its less accurate counterpart if it exists.

### 4.4.2 Synchronization Function

```c
void __syncthreads();
```
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synchronizes all threads in a block. Once all threads have reached this point, execution resumes normally.

__syncthreads() is used to coordinate communication between the threads of a same block. When some threads within a block access the same addresses in shared or global memory, there are potential read-after-write, write-after-read, or write-after-write hazards for some of these memory accesses. These data hazards can be avoided by synchronizing threads in-between these accesses.

__syncthreads() is allowed in conditional code but only if the conditional evaluates identically across the entire thread block, otherwise the code execution is likely to hang or produce unintended side effects.

### 4.4.3 Type Casting Functions

```cpp
float __int_as_float(int);
```

performs a floating-point type cast on the integer argument, leaving the value unchanged. For example, `__int_as_float(0xC0000000)` is equal to `-2`.

```cpp
int __float_as_int(float);
```

performs an integer type cast on the floating-point argument, leaving the value unchanged. For example, `__float_as_int(1.0f)` is equal to `0x3f800000`.

### 4.4.4 Texture Functions

```cpp
template<class Type>
Type texfetch(texture<Type, 1, cudaReadModeElementType> texRef, int x);

template<class Type>
Type texfetch(texture<Type, 2, cudaReadModeElementType> texRef, int x, int y);

template<class Type>
fType texfetch(texture<Type, 1, cudaReadModeNormalizedFloat> texRef, int x);

template<class Type>
fType texfetch(texture<Type, 2, cudaReadModeNormalizedFloat> texRef, int x, int y);

template<class Type>
OutputType texfetch(texture<Type, Dim, ReadMode> texRef, float x);

template<class Type>
OutputType texfetch(texture<Type, Dim, ReadMode> texRef, float x, float y);

template<class Type>
OutputType texfetch(texture<Type, Dim, ReadMode> texRef, float2 xy);
```

fetch the texture bound to texture reference `texRef` using texture coordinates `x`, `y`, or `xy`. `OutputType` is either equal to `Type`, or equal to `float`, `float2`, or
**float4.** If `OutputType` is a floating-point type and `Type` is an integer type, the full range of the integer type is mapped to \([0, 1]\); for example, an unsigned 8-bit texture element with the value 0xff reads as 1.

```cpp
template<class Type>
Type texfetch(texture<Type, Dim, ReadMode> texRef, int x)
```
fetches the texture bound to texture reference `texRef` using texture coordinate `x`.

### 4.5 Host Runtime Component

The host runtime component can only be used by host functions.

It provides functions to handle:

- Device management,
- Context management,
- Memory management,
- Code module management,
- Execution control,
- Texture reference management,
- Interoperability with OpenGL and Direct3D.

It is composed of two APIs:

- A low-level API called the **CUDA driver API**,
- A higher-level API called the **CUDA runtime API** that is implemented on top of the CUDA driver API.

These APIs are mutually exclusive: An application should use either one or the other.

The CUDA runtime eases device code management by providing implicit initialization, context management, and module management. The C host code generated by `nvcc` is based on the CUDA runtime (see Section 4.2.5), so applications that link to this code must use the CUDA runtime API.

In contrast, the CUDA driver API requires more code, is harder to program and debug, but offers a better level of control and is language-independent since it only deals with `cubin` objects (see Section 4.2.5). In particular, it is more difficult to configure and launch kernels using the CUDA driver API, since the execution configuration and kernel parameters must be specified with explicit function calls instead of the execution configuration syntax described in Section 4.2.3. Also, device emulation (see Section 4.5.2.8) does not work with the CUDA driver API.

The CUDA driver API is delivered through the `cuda` dynamic library and all its entry points are prefixed with `cu`.

The CUDA runtime API is delivered through the `cudart` dynamic library and all its entry points are prefixed with `cuda`.
4.5.1 Common Concepts

4.5.1.1 Device
Both APIs provide a way to enumerate the devices available on the system, query their properties, and select one of them for kernel executions.

One property of a device is its *compute capability* defined as a major revision number and a minor revision number. In this version of CUDA, the major revision number is 1 and the minor revision number is 0.

4.5.1.2 Memory
Device memory can be allocated either as *linear memory* or as *arrays*.

Linear memory exists on the device in a 32-bit address space, so separately allocated entities can reference one another via pointers, for example, in a binary tree.

Arrays are opaque memory layouts optimized for texture fetching. They are one-dimensional or two-dimensional and composed of elements, each of which has 1, 2 or 4 components that may be signed or unsigned 8-, 16- or 32-bit integers, 16-bit floats (CUDA driver only), or 32-bit floats. Arrays are only readable by kernels through texture fetching.

Both linear memory and arrays are only readable and writable by the host through the memory copy functions described in Sections 4.5.2.2 and 4.5.3.5.

4.5.1.3 Texture
Both linear memory and arrays can be bound to texture references (see Section 4.3.4) and several distinct texture references might be bound to the same texture or to textures that overlap in memory.

Device memory reads through texture fetching present several advantages over reads from global or constant memory:

- They are cached (see Section 6.1.2.3),
- They are not subject to the constraints on memory access patterns that global or constant memory reads must respect to get good performance (see Sections 6.1.2.1 and 6.1.2.2);
- The latency of addressing calculations is hidden better, possibly improving performance for applications that perform random accesses to the data;
- Packed data may be broadcast to separate variables in a single operation.

If the texture is an array, there are other advantages (see Sections 4.3.4 and 4.5.3.6):

- Integer and 16-bit floating-point input data may be optionally converted to 32-bit floating-point values in the range [0, 1];
- There are several addressing modes available for edge cases;
- They can be optionally filtered.

These last features are not supported for texture in linear memory as mentioned in Section 4.3.4.

Arrays may only be bound to texture references with the same number of packed components.
4.5.1.4 OpenGL Interoperability
OpenGL buffer objects may be mapped into the address space of CUDA, either to enable CUDA to read data written by OpenGL or to enable CUDA to write data for consumption by OpenGL.

4.5.1.5 Direct3D Interoperability
Direct3D 9.0 vertex buffers may be mapped into the address space of CUDA, either to enable CUDA to read data written by Direct3D or to enable CUDA to write data for consumption by Direct3D.

A CUDA context may interoperate with only one Direct3D device at a time, bracketed by calls to the begin/end functions described in Sections 4.5.2.6 and 4.5.3.9.

CUDA does not yet support:
- Versions other than Direct3D 9.0,
- Direct3D objects other than vertex buffers,
- Mapping of more than one vertex buffers simultaneously.

4.5.2 Runtime API
There is no explicit initialization function for the runtime API; it initializes the first time a runtime function is called. One needs to keep this in mind when timing runtime function calls and when interpreting the error code from the first call into the runtime.

By design, a host thread can execute device code on only one device. As a consequence, multiple host threads are required to execute device code on multiple devices.

The functions from Section 4.5.2.1 provide a way to enumerate the devices present in the system and to select one as the device associated to the host thread using `cudaSetDevice()`. A device must be selected before any `__global__` function or any function from Sections 4.5.2.2, 4.5.2.3, 4.5.2.5, 4.5.2.6, and 4.5.2.7 is called; otherwise, device 0 is automatically selected and any subsequent device selection will have no effect.

4.5.2.1 Device Management
`cudaError_t cudaGetDeviceCount(int* count);`
returns in *count* the number of devices currently available for execution.

`cudaError_t cudaGetDeviceProperties(struct cudaDeviceProp* prop, int dev);`
returns in *prop* the properties of device *dev*. The `cudaDeviceProp` structure is defined as:

```c
cstruct cudaDeviceProp {
    char*  name;
    size_t bytes;
    int    major;
    int    minor;
};
```
where:
- **name** is an ASCII string identifying the device;
- **bytes** is the total amount of memory available on the device in bytes;
- **major** and **minor** are the major and minor revision numbers.

```c
cudaError_t cudaChooseDevice(int* dev,
    const struct cudaDeviceProp& prop);
```
returns in *dev the device which properties best match *prop.

```c
cudaError_t cudaSetDevice(int dev);
```
records dev as the device on which the active host thread executes the device code.

```c
cudaError_t cudaGetDevice(int* dev);
```
returns in *dev the device on which the active host thread executes the device code.

### 4.5.2.2 Memory Management

```c
cudaError_t cudaMalloc(void** devPtr, size_t count);
```
allocates count bytes of linear memory on the device and returns in *devPtr a pointer to the allocated memory. The allocated memory is suitably aligned for any kind of variable. The memory is not cleared. `cudaMalloc()` returns `cudaErrorMemoryAllocationFailed` in case of failure.

```c
CUresult cudaMalloc2D(void** devPtr, unsigned int* pitch,
    unsigned int widthInBytes, unsigned int height);
```
allocates at least widthInBytes*height bytes of linear memory on the device and returns in *devPtr a pointer to the allocated memory. The function may pad the allocation to ensure that corresponding pointers in any given row will continue to meet the alignment requirements for coalescing as the address is updated from row to row (see Section 6.1.2.1). The pitch returned in *pitch by `cudaMalloc2D()` is the width in bytes of the allocation. The intended usage of pitch is as a separate parameter of the allocation, used to compute addresses within the 2D array. Given the row and column of an array element of type T, the address is computed as

\[
T* pElement = (T*)((char*)BaseAddress + Row * pitch) + Column;
\]

For allocations of 2D arrays, it is recommended that developers consider performing pitch allocations using `cudaMalloc2D()`. Due to pitch alignment restrictions in the hardware, this is especially true if the application will be performing 2D memory copies between different regions of device memory (whether linear memory or arrays).

```c
cudaError_t cudaFree(void* devPtr);
```
frees the memory space pointed to by devPtr, which must have been returned by a previous call to `cudaMalloc()` or `cudaMalloc2D()`. Otherwise, or if `cudaFree(devPtr)` has already been called before, an error is returned. If devPtr is 0, no operation is performed. `cudaFree()` returns `cudaErrorMemoryFreeFailed` in case of failure.

```c
cudaError_t cudaMallocArray(struct cudaArray** array,
    const struct cudaChannelFormatDesc* desc,
    size_t width, size_t height);
```
allocates an array according to the `cudaChannelFormatDesc` structure `desc` and returns a handle to the new array in `*array`. `cudaChannelFormatDesc` is described in Section 4.3.4.

```c
cudaError_t cudaFreeArray(struct cudaArray* array);
```

frees the array `array`.

```c
cudaError_t cudaMemcpy(void* devPtr, int value, size_t count);
```

fills the first `count` bytes of the memory area pointed to by `devPtr` with the constant byte value `value`.

```c
cudaError_t cudaMemcpy2D(void* dstPtr, size_t pitch, int value, size_t width, size_t height);
```

sets to the specified value `value` a matrix (height rows of width bytes each) pointed to by `dstPtr`. `pitch` is the pitch in the memory area pointed to by `dstPtr`.

```c
cudaError_t cudaMemcpy(void* dst, const void* src, size_t count, enum cudaMemcpyKind kind);
```

copies `count` bytes from the memory area pointed to by `src` to the memory area pointed to by `dst`, where `kind` is one of `cudaMemcpyHostToHost`, `cudaMemcpyHostToDevice`, `cudaMemcpyDeviceToHost`, or `cudaMemcpyDeviceToDevice`, and specifies the direction of the copy. The memory areas may not overlap. Calling `cudaMemcpy()` with `dst` and `src` pointers that do not match the direction of the copy results in an undefined behavior.

```c
cudaError_t cudaMemcpy2D(void* dst, size_t dpitch, const void* src, size_t spitch, size_t width, size_t height, enum cudaMemcpyKind kind);
```

copies a matrix (height rows of width bytes each) from the memory area pointed to by `src` to the memory area pointed to by `dst`, where `kind` is one of `cudaMemcpyHostToHost`, `cudaMemcpyHostToDevice`, `cudaMemcpyDeviceToHost`, or `cudaMemcpyDeviceToDevice`, and specifies the direction of the copy. `dpitch` and `spitch` are the pitch in the memory areas pointed to by `dst` and `src`. The memory areas may not overlap. Calling `cudaMemcpy2D()` with `dst` and `src` pointers that do not match the direction of the copy results in an undefined behavior.

```c
cudaError_t cudaMemcpyToArray(struct cudaArray* dstArray, size_t dstX, size_t dstY, const void* src, size_t count, enum cudaMemcpyKind kind);
```

copies `count` array elements from the memory area pointed to by `src` to the array `dstArray` starting at the upper left corner (`dstX, dstY`), where `kind` is one of `cudaMemcpyHostToHost`, `cudaMemcpyHostToDevice`, `cudaMemcpyDeviceToHost`, or `cudaMemcpyDeviceToDevice`, and specifies the direction of the copy.
copies a matrix (height rows of width bytes each) from the memory area pointed to by src to the array dstArray starting at the upper left corner (dstX, dstY), where kind is one of cudaMemcpyHostToHost, cudaMemcpyHostToDevice, cudaMemcpyDeviceToHost, or cudaMemcpyDeviceToDevice, and specifies the direction of the copy. \textbf{spitch} is the pitch in the memory area pointed to by src.

\begin{verbatim}
cudaError_t cudaMemcpyFromArray(void* dst, 
    const struct cudaArray* srcArray, 
    size_t srcX, size_t srcY, 
    size_t count, 
    enum cudaMemcpyKind kind);
\end{verbatim}

copies \textbf{count} bytes from the array \textbf{srcArray} starting at the upper left corner \textbf{(srcX, srcY)} to the memory area pointed to by \textbf{dst}, where kind is one of cudaMemcpyHostToHost, cudaMemcpyHostToDevice, cudaMemcpyDeviceToHost, or cudaMemcpyDeviceToDevice, and specifies the direction of the copy.

\begin{verbatim}
cudaError_t cudaMemcpy2DFromArray(void* dst, size_t dpitch, 
    const struct cudaArray* srcArray, 
    size_t srcX, size_t srcY, 
    size_t width, size_t height, 
    enum cudaMemcpyKind kind);
\end{verbatim}

copies a matrix (height rows of width bytes each) from the array \textbf{srcArray} starting at the upper left corner \textbf{(srcX, srcY)} to the memory area pointed to by \textbf{dst}, where kind is one of cudaMemcpyHostToHost, cudaMemcpyHostToDevice, cudaMemcpyDeviceToHost, or cudaMemcpyDeviceToDevice, and specifies the direction of the copy. \textbf{dpitch} is the pitch in the memory area pointed to by \textbf{dst}.

\begin{verbatim}
cudaError_t cudaMemcpyArrayToArray(struct cudaArray* dstArray, 
    size_t dstX, size_t dstY, 
    const struct cudaArray* srcArray, 
    size_t srcX, size_t srcY, 
    size_t count, 
    enum cudaMemcpyKind kind);
\end{verbatim}

copies \textbf{count} bytes from the array \textbf{srcArray} starting at the upper left corner \textbf{(srcX, srcY)} to the array \textbf{dstArray} starting at the upper left corner \textbf{(dstX, dstY)}, where kind is one of cudaMemcpyHostToHost, cudaMemcpyHostToDevice, cudaMemcpyDeviceToHost, or cudaMemcpyDeviceToDevice, and specifies the direction of the copy.

\begin{verbatim}
cudaError_t cudaMemcpy2DArrayToArray(struct cudaArray* dstArray, 
    size_t dstX, size_t dstY, 
    const struct cudaArray* srcArray, 
    size_t srcX, size_t srcY, 
    size_t width, size_t height, 
    enum cudaMemcpyKind kind);
\end{verbatim}

copies a matrix (height rows of width bytes each) from the array \textbf{srcArray} starting at the upper left corner \textbf{(srcX, srcY)} to the array \textbf{dstArray} starting at the upper left corner \textbf{(dstX, dstY)}, where kind is one of cudaMemcpyHostToHost, cudaMemcpyHostToDevice, cudaMemcpyDeviceToHost, or cudaMemcpyDeviceToDevice, and specifies the direction of the copy.

\begin{verbatim}
template<class T>
\end{verbatim}
cudaError_t cudaMemcpyToSymbol(const T& symbol, const void* src, size_t count, size_t offset = 0);

copies count bytes from the memory area pointed to by src to the memory area pointed to by offset bytes from the start of symbol symbol. The memory areas may not overlap. symbol can either be a variable that resides in global memory space, or it can be a character string, naming a variable that resides in global memory space. cudaMemcpyToSymbol() always copies data from the host to the device.

template<class T>
cudaError_t cudaMemcpyFromSymbol(void *dst, const T& symbol, size_t count, size_t offset = 0);

copies count bytes from the memory area pointed to by offset bytes from the start of symbol symbol to the memory area pointed to by dst. The memory areas may not overlap. symbol can either be a variable that resides in global memory space, or it can be a character string, naming a variable that resides in global memory space. cudaMemcpyFromSymbol() always copies data from the device to the host.

template<class T>
cudaError_t cudaMemcpyFromSymbol(void *dst, const T& symbol, size_t count, size_t offset = 0);

copies count bytes from the memory area pointed to by offset bytes from the start of symbol symbol to the memory area pointed to by dst. The memory areas may not overlap. symbol can either be a variable that resides in global memory space, or it can be a character string, naming a variable that resides in global memory space. cudaMemcpyFromSymbol() always copies data from the device to the host.

template<class T>
cudaError_t cudaMemcpyFromSymbol(void *dst, const T& symbol, size_t count, size_t offset = 0);

copies count bytes from the memory area pointed to by offset bytes from the start of symbol symbol to the memory area pointed to by dst. The memory areas may not overlap. symbol can either be a variable that resides in global memory space, or it can be a character string, naming a variable that resides in global memory space. cudaMemcpyFromSymbol() always copies data from the device to the host.

struct cudaChannelFormatDesc
cudaCreateChannelDesc(int x, int y, int z, int w, enum cudaChannelFormatKind f);

returns a channel descriptor with format f and number of bits of each component x, y, z, and w. cudaChannelFormatDesc is described in Section 4.3.4.

cudaError_t cudaGetChannelDesc(struct cudaChannelFormatDesc* desc, const struct cudaArray* array);

returns in *desc the channel descriptor of array array.

cudaError_t cudaBindTexture(const char* symbol, const void* devPtr, const struct cudaChannelFormatDesc* desc, size_t size, size_t offset);
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binds the memory area of size size pointed to by (devPTr + offset) to the texture reference defined by symbol symbol.desc describes the format of the value returned when fetching the texture.

cudaError_t cudaBindTexture(const char* symbol,
                         const struct cudaArray* array,
                         const struct cudaChannelFormatDesc* desc);

binds the array array to the texture reference defined by symbol symbol.desc supersedes the channel descriptor associated to array array.

cudaError_t cudaUnbindTexture(const char* symbol);

unbinds the texture bound to the texture reference defined by symbol symbol.

cudaError_t cudaGetTextureReference(
                        struct textureReference** texRef,
                        const char* symbol);

returns in *textureReference the structure associated to the texture reference defined by symbol symbol.

4.5.2.4 Execution Control

Kernels are invoked using the execution configuration syntax described in Section 4.2.3. This syntax is only available in source code compiled with nvcc (see Section 4.2.5). The functions described in this section provide a way to invoke kernels from source code that is not compiled with nvcc.

cudaError_t cudaConfigureCall(dim3 gridDim, dim3 blockDim,
                         size_t sharedMem = 0,
                         int tokens = 0);

specifies the grid and block dimensions for the device call to be executed similar to the execution configuration syntax described in Section 4.2.3. cudaConfigureCall() is stack based. Each call pushes data on top of an execution stack. This data contains the dimension for the grid and thread blocks, together with any arguments for the call.

template<class T> cudaError_t cudaLaunch(T entry);

launches the function entry on the device. entry can either be a function that executes on the device, or it can be a character string, naming a function that executes on the device. entry must be declared as a __global__ function. cudaLaunch() must be preceded by a call to cudaConfigureCall() since it pops the data that was pushed by cudaConfigureCall() from the execution stack.

cudaError_t cudaSetupArgument(void* arg,
                        size_t count, size_t offset);

template<class T> cudaError_t cudaSetupArgument(T arg,
                        size_t offset);

pushes count bytes of the argument pointed to by arg at offset bytes from the start of the parameter passing area, which starts at offset 0. The arguments are stored in the top of the execution stack. cudaSetupArgument() must be preceded by a call to cudaConfigureCall().

4.5.2.5 OpenGL Interoperability

cudaError_t cudaGLRegisterBufferObject(GLuint bufferObj);
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registers the buffer object of ID `bufferObj` for access by CUDA. This function must be called before CUDA can map the buffer object. While it is registered, the buffer object cannot be used by any OpenGL commands except as a data source for OpenGL drawing commands.

```c
cudaError_t cudaMapBufferObject(void** devPtr,
                                 unsigned int* size,
                                 GLuint bufferObj);
```
maps the buffer object of ID `bufferObj` into the address space of CUDA and returns in `*devPtr` and `*size` the base pointer and size of the resulting mapping.

```c
cudaError_t cudaGLUnmapBufferObject(GLuint bufferObj);
```
unmaps the buffer object of ID `bufferObj` for access by CUDA.

```c
cudaError_t cudaGLUnregisterBufferObject(GLuint bufferObj);
```
unregisters the buffer object of ID `bufferObj` for access by CUDA.

### 4.5.2.6 Direct3D Interoperability

```c
cudaError_t cudaD3D9Begin(IDirect3DDevice9* device);
```
initializes interoperability with the Direct3D device `device`. This function must be called before CUDA can map any objects from `device`. The application can then map vertex buffers owned by the Direct3D device until `cudaD3D9End()` is called.

```c
cudaError_t cudaD3D9End();
```
concludes interoperability with the Direct3D device previously specified to `cudaD3D9Begin()`.

```c
cudaError_t cudaD3D9RegisterVertexBuffer(IDirect3DVertexBuffer9* VB);
```
registers the Direct3D vertex buffer `VB` for access by CUDA.

```c
cudaError_t cudaD3D9MapVertexBuffer(void** devPtr,
                                     unsigned int* size,
                                     IDirect3DVertexBuffer9* VB);
```
maps the Direct3D vertex buffer `VB` into the address space of the current CUDA context and returns in `*devPtr` and `*size` the base pointer and size of the resulting mapping.

```c
cudaError_t cudaD3D9UnmapVertexBuffer(IDirect3DVertexBuffer9* VB);
```
unmaps the vertex buffer `VB` for access by CUDA.

### 4.5.2.7 Error Handling

```c
cudaError_t cudaGetLastError(void);
```
returns the last error that was returned from any of the runtime calls in the same host thread and resets it to `cudaSuccess`.

```c
const char* cudaGetErrorString(cudaError_t error);
```
returns a message string from an error code.

### 4.5.2.8 Debugging using the Device Emulation Mode

The programming environment does not include any native debug support for code that runs on the device, but comes with a device emulation mode for the purpose of debugging. When compiling an application in this mode (using the `deviceemu` option), the device code is compiled for and runs on the host, allowing the developer to use the host’s native debugging support to debug the application as if it
were a host application. The preprocessor macro **DEVICE_EMULATION** is defined in this mode.

When running an application in device emulation mode, the programming model is emulated by the runtime. For each thread in a thread block, the runtime creates a thread on the host. The developer needs to make sure that:

- The host is able to run up to the maximum number of threads per block, plus one for the master thread.
- Enough memory is available to run all threads, knowing that each thread gets 256 KB of stack.

Many features provided through the device emulation mode make it a very effective debugging tool:

- By using the host’s native debugging support developers can use all features that the debugger supports, like setting breakpoints and inspecting data.
- Since device code is compiled to run on the host, the code can be augmented with code that cannot run on the device, like input and output operations to files or to the screen (`printf()`, etc.).
- Since all data resides on the host, any device- or host-specific data can be read from either device or host code; similarly, any device or host function can be called from either device or host code.
- In case of incorrect usage of the synchronization intrinsic, the runtime detects deadlock situations.

Developers must keep in mind that device emulation mode is emulating the device, not simulating it. Therefore, device emulation mode is very useful in finding algorithmic errors, but certain errors are hard to find:

- When a memory location is accessed in multiple threads within the grid at potentially the same time, the results when running in device emulation mode potentially differ from the results when running on the device, since in emulation mode threads execute sequentially.
- When dereferencing a pointer to global memory on the host or a pointer to host memory on the device, device execution almost certainly fails in some undefined way, whereas device emulation can produce correct results.
- Most of the time the same floating-point computation will not produce exactly the same result when performed on the device as when performed on the host in device emulation mode. This is expected since in general, all you need to get different results for the same floating-point computation are slightly different compiler options, let alone different compilers, different instruction sets, or different architectures.

In particular, some host platforms store intermediate results of single-precision floating-point calculations in extended precision registers, potentially resulting in significant differences in accuracy when running in device emulation mode.

When this occurs, developers can try any of the following methods, none of which is guaranteed to work:

- Declare some floating-point variables as volatile to force single-precision storage;
- Use the `-ffloat-store` compiler option of `gcc`,
- Use the `/Op` or `/fp` compiler options of the Visual C++ compiler,
> Use the _controlfp() run-time function provided by the Visual C++
compiler to control floating-point precision, rounding, and infinity modes
for portions of the code; to force single-precision floating-point
computation for a portion of the code, one would first get the current
control word and save it using

```c
unsigned int originalCW = _controlfp(0, 0);
```
then change the control word to force the mantissa to be stored in 24 bits
using

```c
_controlfp(_PC_24, _MCW_PC);
```
and finally restore the original control word using

```c
_controlfp(originalCW, 0xfffff);
```

Unlike the GeForce 8800 Series (see Section 5.2), host platforms also usually
support denormalized numbers. This can lead to dramatically different results
between device emulation and device execution modes since some computation
might produce a finite result in one case and an infinite result in the other.

### 4.5.3 Driver API

The driver API is a handle-based, imperative API: Most objects are referenced by
opaque handles that may be specified to functions to manipulate the objects.

The objects available in CUDA are summarized in Table 4-1.

<table>
<thead>
<tr>
<th>Object</th>
<th>Handle</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Device</td>
<td>CUdevice</td>
<td>CUDA-capable device</td>
</tr>
<tr>
<td>Context</td>
<td>N/A</td>
<td>Roughly equivalent to a CPU process</td>
</tr>
<tr>
<td>Module</td>
<td>CUmodule</td>
<td>Roughly equivalent to a dynamic library</td>
</tr>
<tr>
<td>Function</td>
<td>CUfunction</td>
<td>Kernel</td>
</tr>
<tr>
<td>Heap memory</td>
<td>CUdeviceptr</td>
<td>Pointer to device memory</td>
</tr>
<tr>
<td>Array</td>
<td>CUarray</td>
<td>Opaque container for 1D or 2D data on the device, readable via texture references</td>
</tr>
<tr>
<td>Texture reference</td>
<td>CUtexref</td>
<td>Object that describes how to interpret texture memory data</td>
</tr>
</tbody>
</table>

#### 4.5.3.1 Initialization

```c
CUresult cuInit(void);
```
initializes the driver API and must be called before any other function from the
driver API. If `cuInit()` has not been called, any function from the driver API will return `CUDA_ERROR_NOT_INITIALIZED`.

#### 4.5.3.2 Devices

```c
CUresult cuDeviceGetCount(int* count);
```
returns in `*count` the number of devices currently available for execution.

```c
CUresult cuDeviceGet(CUdevice* dev, int ordinal);
```
returns in *dev a device handle given an ordinal in the range
[0, cuDeviceGetCount() -1].

CUresult cuDeviceGetName(char* name, int len, CUdevice dev);
returns an ASCII string identifying the device dev in the NULL-terminated string
pointed to by name. len specifies the maximum length of the string that may be
returned.

CUresult cuDeviceTotalMem(unsigned int* bytes, CUdevice dev);
returns in *bytes the total amount of memory available on the device dev in
bytes.

CUresult cuDeviceComputeCapability(int* major, int* minor,
CUdevice dev);
returns in *major and *minor the the major and minor revision numbers of
device dev.

4.5.3.3 Context Management
A CUDA context is analogous to a CPU process. All resources and actions
performed within the compute API are encapsulated inside a CUDA context, and
the system automatically cleans up these resources when the context is destroyed.
Besides objects such as modules and texture references, each context has its own
distinct 32-bit address space. As a result, CUdeviceptr values from different
CUDA contexts reference different memory locations.

Contexts have a one-to-one correspondence with host threads. A host thread may
have only one device context current at a time. For this reason, device contexts are
not explicitly referenced by handle. When a context is created, it is made current to
the calling host thread and its thread affiliation cannot be changed.

CUDA functions that operate in a context (most functions that do not involve
device enumeration or context management) will return
CUDA_ERROR_INVALID_CONTEXT if a valid context is not current to the thread.

To facilitate interoperability between third party authored code operating in the
same context, the driver API maintains a usage count that is incremented by each
distinct client of a given context. For example, if three libraries are loaded to use the
same CUDA context, each library must call cuCtxAttach() to increment the
usage count and cuCtxDetach() to decrement the usage count when the library is
done using the context. The context is destroyed when the usage count goes to 0.
For most libraries, it is expected that the application will have created a CUDA
context before loading or initializing the library; that way, the application can create
the context using its own heuristics, and the library simply operates on the context
handed to it.

CUresult cuCtxCreate(CUdevice dev);
creates a new context for a device and associates it with the calling thread. The
context is created with a usage count of 1 and the caller of cuCtxCreate() must
call cuCtxDetach() when done using the context. This function fails if a context
is already current to the thread.

CUresult cuCtxAttach(void);
increments the usage count of the context. This function fails if there is no context
current to the thread.

CUresult cuCtxDetach(void);
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decrements the usage count of the context, and destroys the context if the usage count goes to 0.

4.5.3.4 Module Management

Modules are dynamically loadable packages of device code and data, akin to DLLs in Windows. The names for all symbols, including functions, global variables, and texture references, are maintained at module scope so that modules written by independent third parties may interoperate in the same CUDA context.

`CUresult cuModuleLoad(CUmodule* mod, const char* filename);` takes a file name `filename` and loads the corresponding module `mod` into the current context. The CUDA driver API does not attempt to lazily allocate the resources needed by a module; if the memory for functions and data (constant and global) needed by the module cannot be allocated, `cuModuleLoad()` fails. The file should be a `cubin` file as output by `nvcc` (see Section 4.2.5).

`CUresult cuModuleLoadData(CUmodule* mod, const void* image);` takes a pointer `image` and loads the corresponding module `mod` into the current context. The pointer may be obtained by mapping a `cubin` file, passing a `cubin` file as a text string, or incorporating a `cubin` object into the executable resources and using operation system calls such as Windows’ `FindResource()` to obtain the pointer.

`CUresult cuModuleUnload(CUmodule mod);` unloads a module `mod` from the current context.

`CUresult cuModuleGetFunction(CUfunction* func,` returns in `*func` the handle of the function of name `funcname` located in module `mod`. If no function of that name exists, `cuModuleGetFunction()` returns `CUDA_ERROR_NOT_FOUND`.

`CUresult cuModuleGetGlobal(CUdeviceptr* devPtr,` returns in `*devPtr` and `*bytes` the base pointer and size of the global of name `globalname` located in module `mod`. If no variable of that name exists, `cuModuleGetGlobal()` returns `CUDA_ERROR_NOT_FOUND`. Both parameters `ptr` and `bytes` are optional. If one of them is null, it is ignored.

`CUresult cuModuleGetTexRef(CUtexref* texRef,` returns in `*texref` the handle of the texture reference of name `texrefname` in the module `mod`. If no texture reference of that name exists, `cuModuleGetTexRef()` returns `CUDA_ERROR_NOT_FOUND`.

4.5.3.5 Memory Management

`CUresult cuMemAlloc(CUdeviceptr* devPtr, unsigned int count);` allocates `count` bytes of linear memory on the device and returns in `*devPtr` a pointer to the allocated memory. The allocated memory is suitably aligned for any kind of variable. The memory is not cleared. If `count` is 0, `cuMemAlloc()` returns `CUDA_ERROR_INVALID_VALUE`.

`CUresult cuMemAlloc2D(CUdeviceptr* devPtr,` allocates memory in a 2D array layout.
allocates at least \texttt{widthInBytes*height} bytes of linear memory on the device and returns in \texttt{*devPtr} a pointer to the allocated memory. The function may pad the allocation to ensure that corresponding pointers in any given row will continue to meet the alignment requirements for coalescing as the address is updated from row to row (see Section 6.1.2.1). \texttt{elementSizeBytes} specifies the size of the largest reads and writes that will be performed on the memory range. \texttt{elementSizeBytes} may be 4, 8 or 16 (since coalesced memory transactions are not possible on other data sizes). If \texttt{elementSizeBytes} is smaller than the actual read/write size of a kernel, the kernel will run correctly, but possibly at reduced speed. The pitch returned in \texttt{*pitch} by \texttt{cuMemAlloc2D()} is the width in bytes of the allocation. The intended usage of pitch is as a separate parameter of the allocation, used to compute addresses within the 2D array. Given the row and column of an array element of type \texttt{T}, the address is computed as

\[
T* pElement = (T*)((char*)BaseAddress + Row * Pitch) + Column;
\]

The pitch returned by \texttt{cuMemAlloc2D()} is guaranteed to work with \texttt{cuMemcpy2D()} under all circumstances. For allocations of 2D arrays, it is recommended that developers consider performing pitch allocations using \texttt{cuMemAlloc2D()}. Due to pitch alignment restrictions in the hardware, this is especially true if the application will be performing 2D memory copies between different regions of device memory (whether linear memory or arrays).

\texttt{CUresult cuMemFree(CUdeviceptr devPtr);} frees the memory space pointed to by \texttt{devPtr}, which must have been returned by a previous call to \texttt{cudaMalloc()} or \texttt{cudaMalloc2D()}.

\texttt{CUresult cuMemGetAddressRange(CUdeviceptr* basePtr, unsigned int* size, CUdeviceptr devPtr);} returns the base address in \texttt{*basePtr} and size and \texttt{*size} of the allocation by \texttt{cuMemAlloc()} or \texttt{cuMemAlloc2D()} that contains the input pointer \texttt{devPtr}. Both parameters \texttt{basePtr} and \texttt{size} are optional. If one of them is null, it is ignored.

\texttt{CUresult cuArrayCreate(CUarray* array, const CUDA_ARRAY_DESCRIPTOR* desc);} creates an array according to the \texttt{CUDA_ARRAY_DESCRIPTOR} structure \texttt{desc} and returns a handle to the new array in \texttt{*array}. The \texttt{CUDA_ARRAY_DESCRIPTOR} structure is defined as such:

\[
\text{typedef struct} \{ \\
\text{unsigned int Width;} \\
\text{unsigned int Height;} \\
\text{CUarray_format Format;} \\
\text{unsigned int NumPackedComponents;} \\
\} \text{CUDA_ARRAY_DESCRIPTOR;}
\]

where:

\begin{itemize}
\item \textbf{Width} and \textbf{Height} are the width and height of the array (in elements);
\item \textbf{NumPackedComponents} specifies the number of packed components per array element; it may be 1, 2 or 4;
\end{itemize}
Format specifies the format of the elements; CUarray_format is defined as such:

```c
typedef enum CUarray_format_enum {
    CU_AD_FORMAT_UNSIGNED_INT8  = 0x01,
    CU_AD_FORMAT_UNSIGNED_INT16 = 0x02,
    CU_AD_FORMAT_UNSIGNED_INT32 = 0x03,
    CU_AD_FORMAT_SIGNED_INT8    = 0x08,
    CU_AD_FORMAT_SIGNED_INT16   = 0x09,
    CU_AD_FORMAT_SIGNED_INT32   = 0x0a,
    CU_AD_FORMAT_HALF           = 0x10,
    CU_AD_FORMAT_FLOAT          = 0x20
} CUarray_format;
```

Here are examples of array descriptions:

- **Description for an array of 2048 floats:**
  ```c
  CUDA_ARRAY_DESCRIPTOR desc;
  desc.Format = CU_AD_FORMAT_FLOAT;
  desc.NumPackedComponents = 1;
  desc.Width = 2048;
  desc.Height = 1;
  ```

- **Description for a 64×64 array of floats:**
  ```c
  CUDA_ARRAY_DESCRIPTOR desc;
  desc.Format = CU_AD_FORMAT_FLOAT;
  desc.NumPackedComponents = 1;
  desc.Width = 64;
  desc.Height = 64;
  ```

- **Description for a width×height array of 64-bit, 4x16-bit float16's:**
  ```c
  CUDA_ARRAY_DESCRIPTOR desc;
  desc.FormatFlags = CU_AD_FORMAT_HALF;
  desc.NumPackedComponents = 4;
  desc.Width = width;
  desc.Height = height;
  ```

- **Description for a width×height array of 16-bit elements, each of which is two 8-bit unsigned chars:**
  ```c
  CUDA_ARRAY_DESCRIPTOR arrayDesc;
  desc.FormatFlags = CU_AD_FORMAT_UNSIGNED_INT8;
  desc.NumPackedComponents = 2;
  desc.Width = width;
  desc.Height = height;
  ```

CUresult cuArrayGetDescriptor(CUDA_ARRAY_DESCRIPTOR* arrayDesc, 
   CUarray array);
returns in *arrayDesc the descriptor that was used to create the array array. It is useful for subroutines that have been passed an array, but need to know the array parameters for validation or other purposes.

CUresult cuArrayDestroy(CUarray array);
destroys the array array.

CUresult cuMemsetD8(CUdeviceptr dstDevice, 
   unsigned char value, unsigned int count);
CUresult cuMemsetD16(CUdeviceptr dstDevice, 
   unsigned short value, unsigned int count);
CUresult cuMemsetD32(CUdeviceptr dstDevice, 
   unsigned int value, unsigned int count);
sets the memory range of `count` 8-, 16-, or 32-bit values to the specified value `value`.

```c
CUresult cuMemcpyStoD(CUdeviceptr dstDevPtr, const void *srcHostPtr, unsigned int count);
```
copies from host memory to device memory. `dstDevPtr` and `srcHostPtr` specify the base addresses of the destination and source, respectively. `count` specifies the number of bytes to copy.

```c
CUresult cuMemcpyDtoS(void* dstHostPtr, CUdeviceptr srcDevPtr, unsigned int count);
```
copies from device to host memory. `dstHostPtr` and `srcDevPtr` specify the base addresses of the source and destination, respectively. `count` specifies the number of bytes to copy.

```c
CUresult cuMemcpyDtoD(CUdeviceptr dstDevPtr, CUdeviceptr srcDevPtr, unsigned int count);
```
copies from device memory to device memory. `dstDev` and `srcDevPtr` are the base pointers of the destination and source, respectively. `count` specifies the number of bytes to copy.

```c
CUresult cuMemcpyDtoA(CUarray dstArray, unsigned int dstIndex, CUdeviceptr srcDevPtr, unsigned int count);
```
copies from device memory to an array. `dstArray` and `dstIndex` specify the array handle and starting index of the destination data. `srcDevPtr` specifies the base pointer of the source. `count` specifies the number of bytes to copy.

```c
CUresult cuMemcpyAtoD(CUdeviceptr dstDevPtr, CUarray srcArray, unsigned int srcIndex, unsigned int count);
```
copies from an array to device memory. `dstDevPtr` specifies the base pointer of the destination and must be naturally aligned with the array elements. `srcArray` and `srcIndex` specify the array handle and the index (in array elements) of the array element where the copy is to begin. `count` specifies the number of bytes to copy and must be evenly divisible by the array element size.

```c
CUresult cuMemcpyAtoS(void* dstHostPtr, CUarray srcArray, unsigned int srcIndex, unsigned int count);
```
copies from an array to host memory. `dstHostPtr` specifies the base pointer of the destination. `srcArray` and `srcIndex` specify the array handle and starting index of the source data. `count` specifies the number of bytes to copy.

```c
CUresult cuMemcpyAtoA(CUarray dstArray, unsigned int dstIndex, const void *srcHostPtr, unsigned int count);
```
copies from host memory to an array. `dstArray` and `dstIndex` specify the array handle and starting index of the destination data. `srcHostPtr` specify the base address of the source. `count` specifies the number of bytes to copy.
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copies from one array to another. \texttt{dstArray} and \texttt{srcArray} specify the handles of the destination and source arrays for the copy, respectively. \texttt{dstIndex} and \texttt{srcIndex} specify the destination and source indices into the array. These values are in the range \([0, \text{Width}-1]\) for the array; they are not byte offsets. \texttt{count} is the number of bytes to be copied. The size of the elements in the arrays need not be the same format, but the elements must be the same size; and \texttt{count} must be evenly divisible by that size.

\begin{verbatim}
CUresult cuMemcpy2D(const CUDA_MEMCPY2D* copyParam);
CUresult cuMemcpy2DUnaligned(const CUDA_MEMCPY2D* copyParam);
\end{verbatim}

perform a 2D memory copy according to the parameters specified in \texttt{copyParam}. The \texttt{CUDA_MEMCPY2D} structure is defined as such:

\begin{verbatim}
typedef struct CUDA_MEMCPY2D_st {
  unsigned int srcXInBytes, srcY;
  CUmemorytype srcMemoryType;
  const void *srcSystem;
  CUdeviceptr srcDevice;
  CUarray srcArray;
  unsigned int srcPitch; // ignored when src is array

  unsigned int dstXInBytes, dstY;
  CUmemorytype dstMemoryType;
  void *dstSystem;
  CUdeviceptr dstDevice;
  CUarray dstArray;
  unsigned int dstPitch; // ignored when dst is array

  unsigned int WidthInBytes;
  unsigned int Height;
} CUDA_MEMCPY2D;
\end{verbatim}

where:

- \texttt{srcMemoryType} and \texttt{dstMemoryType} specify the type of memory of the source and destination, respectively; \texttt{CUmemorytype_enum} is defined as such:

\begin{verbatim}
typedef enum CUmemorytype_enum {
  CU_MEMORYTYPE_SYSTEM = 0x01,
  CU_MEMORYTYPE_DEVICE = 0x02,
  CU_MEMORYTYPE_ARRAY = 0x03
} CUmemorytype;
\end{verbatim}

If \texttt{srcMemoryType} is \texttt{CU_MEMORYTYPE_SYSTEM}, \texttt{srcSystem} and \texttt{srcPitch} specify the (system) base address of the source data and the bytes per row to apply. \texttt{srcArray} is ignored.

If \texttt{srcMemoryType} is \texttt{CU_MEMORYTYPE_DEVICE}, \texttt{srcDevice} and \texttt{srcPitch} specify the (device) base address of the source data and the bytes per row to apply. \texttt{srcArray} is ignored.

If \texttt{srcMemoryType} is \texttt{CU_MEMORYTYPE_ARRAY}, \texttt{srcArray} specifies the handle of the source data. \texttt{srcSystem}, \texttt{srcDevice} and \texttt{srcPitch} are ignored.
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If `dstMemoryType` is `CU_MEMORYTYPE_SYSTEM`, `dstSystem` and `dstPitch` specify the (system) base address of the destination data and the bytes per row to apply. `dstArray` is ignored.

If `dstMemoryType` is `CU_MEMORYTYPE_DEVICE`, `dstDevice` and `dstPitch` specify the (device) base address of the destination data and the bytes per row to apply. `dstArray` is ignored.

If `dstMemoryType` is `CU_MEMORYTYPE_ARRAY`, `dstArray` specifies the handle of the destination data. `dstSystem`, `dstDevice` and `dstPitch` are ignored.

- `srcXInBytes` and `srcY` specify the base address of the source data for the copy.
  For system pointers, the starting address is
  ```c
  void* StartSystem = (void*)((char*)srcSystem+srcY*srcPitch + srcXInBytes);
  ```
  For device pointers, the starting address is
  ```c
  CUdeviceptr StartSystem = srcDevice+srcY*srcPitch+srcXInBytes;
  ```
  For arrays, `srcXInBytes` must be evenly divisible by the array element size.

- `dstXInBytes` and `dstY` specify the base address of the destination data for the copy.
  For system pointers, the base address is
  ```c
  void* dstStart = (void*)((char*)dstSystem+dstY*dstPitch + dstXInBytes);
  ```
  For device pointers, the starting address is
  ```c
  CUdeviceptr dstStart = dstDevice+dstY*dstPitch+dstXInBytes;
  ```
  For arrays, `dstXInBytes` must be evenly divisible by the array element size.

- `WidthInBytes` and `Height` specify the width (in bytes) and height of the 2D copy being performed. Any pitches must be greater than or equal to `WidthInBytes`.

`cuMemAlloc2D()` passes back pitches that always work with `cuMemcpy2D()`. On intra-device memory copies (device<--device, array<--device, array<--array), `cuMemcpy2D()` may fail for pitches not computed by `cuMemAlloc2D()`.

`cuMemcpyoutualigned()` does not have this restriction, but may run significantly slower in the cases where `cuMemcpy2D()` would have returned an error code.

### 4.5.3.6 Texture Reference Management

- `CuResult cuModuleGetTexRef(CUtxref* texRef, CUmodule mod, const char* texrefname)` returns in `*texRef` the handle of the texture reference of name `texrefname` that was created when the module `mod` was loaded. This texture reference handle should not be destroyed, since it will be destroyed when the module is unloaded.

- `CuResult cuTexRefCreate(CUtxref* texRef)` creates a texture reference and returns its handle in `*texRef`. Once created, the application must call `cuTexRefSetArray()` or `cuTexRefSetAddress()` to associate the reference with allocated memory. Other texture reference functions
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are used to specify the format and interpretation (addressing, filtering, etc.) to be used when the memory is read through this texture reference. To associate the texture reference with a texture ordinal for a given function, the application should call `cuParamSetTexRef()`.

```c
CUresult cuTexRefDestroy(CUtexref texRef);
```
destroy the texture reference.

```c
CUresult cuTexRefSetArray(CUtexref texRef,
                          CUarray array,
                          unsigned int flags);
```
binds the array `array` to the texture reference `texRef`. Any previous address or array state associated with the texture reference is superseded by this function.

*flags* must be set to `CU_TRSA_OVERRIDE_FORMAT`.

```c
CUresult cuTexRefSetAddress(CUtexref texRef,
                             CUdeviceptr base, CUdeviceptr devPtr,
                             unsigned int bytes);
```
binds a linear address range to the texture reference `texRef`. Any previous address or array state associated with the texture reference is superseded by this function.

```c
CUresult cuTexRefSetFormat(CUtexref texRef,
                           CUarray_format format,
                           unsigned int numPackedComponents);
```
specifies the format of the data to be read by the texture reference `texRef`. *format* and *numPackedComponents* are exactly analogous to the *Format* and *NumPackedComponents* members of the `CUDA_ARRAY_DESCRIPTOR` structure. They specify the format of each component and the number of components per array element.

```c
CUresult cuTexRefSetAddressMode(CUtexref texRef,
                                 unsigned int dim,
                                 CUaddress_mode mode);
```
specifies the addressing mode `mode` for the given dimension of the texture reference `texRef`. If `dim` is zero, the addressing mode is applied to the first parameter of the `texfetch()` function used to fetch from the texture; if `dim` is 1, the second, and so on. `CUaddress_mode` is defined as such:

```c
typedef enum CUaddress_mode_enum {
    CU_TR_ADDRESS_MODE_WRAP = 0,
    CU_TR_ADDRESS_MODE_CLAMP = 1,
    CU_TR_ADDRESS_MODE_MIRROR = 2,
} CUaddress_mode;
```

```c
CUresult cuTexRefSetFilterMode(CUtexref texRef,
                                CUfilter_mode mode);
```
specifies the filtering mode `mode` to be used when reading memory through the texture reference `texRef`. `CUfilter_mode_enum` is defined as such:

```c
typedef enum CUfilter_mode_enum {
    CU_TR_FILTER_MODE_POINT = 0,
    CU_TR_FILTER_MODE_LINEAR = 1,
} CUfilter_mode;
```

```c
CUresult cuTexRefSetFlags(CUtexref texRef, unsigned int Flags);
```
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specifies optional flags to control the behavior of data returned through the texture reference. The valid flags are:

- **CU_TRSF_READ_AS_INTEGER**, which suppresses the default behavior of having the texture promote integer data to floating point data in the range [0, 1];
- **CU_TRSF_NORMALIZED_COORDINATES**, which suppresses the default behavior of having the texture coordinates range from [0, Dim) where Dim is the width or height of the array. Instead, the texture coordinates [0, 1.0) reference the entire breadth of the array dimension.

```c
CUresult cuTexRefGetAddress(CUdeviceptr* baseAddress,
                             CUdeviceptr* pdptr,
                             CUtexref texRef);
```
returns in *baseAddress* the base address bound to the texture reference `texRef`, or returns `CUDA_ERROR_INVALID_VALUE` if the texture reference is not bound to any device memory range.

```c
CUresult cuTexRefGetArray(CUarray* array, CUtexref texRef);
```
returns in *array* the array bound by the texture reference `texRef`, or returns `CUDA_ERROR_INVALID_VALUE` if the texture reference is not bound to any array.

```c
CUresult cuTexRefGetAddressMode(CUaddress_mode* mode,
                                 CUtexref texRef,
                                 unsigned int dim);
```
returns in *mode* the addressing mode corresponding to the dimension `dim` of the texture reference `texRef`. Currently the only valid values for `dim` are 0 and 1.

```c
CUresult cuTexRefGetFilterMode(CUfilter_mode* mode,
                               CUtexref texRef);
```
returns in *mode* the filtering mode of the texture reference `texRef`.

```c
CUresult cuTexRefGetFormat(CUarray_format* format,
                            unsigned int* numPackedComponents,
                            CUtexref texRef);
```
returns in *format* and *numPackedComponents* the format and number of components of the array bound to the texture reference `texRef`. If `format` or `numPackedComponents` is null, it will be ignored.

```c
CUresult cuTexRefGetFlags(unsigned int* flags, CUtexref texRef);
```
returns in *flags* the flags of the texture reference `texRef`.

### 4.5.3.7 Execution Control

The functions described in this section manage the execution of a kernel on the device. **cuFuncSetBlockShape()** sets the number of threads per block for a given function, and how their threadIDs are assigned. **cuFuncSetSharedSize()** sets the size of shared memory for the function. The **cuParam*()** family of functions is used specify the parameters that will be provided to the kernel the next time **cuLaunch()** is invoked.

```c
CUresult cuFuncSetBlockShape(CUfunction func,
                             unsigned int x,
                             unsigned int y,
                             unsigned int z);
```
specifies the X, Y and Z dimensions of the thread blocks that are created when the kernel given by `func` is launched.

```c
CUresult cuFuncSetSharedSize(CUfunction func, unsigned int int bytes);
```
sets through bytes the amount of shared memory that will be available to each thread block when the kernel given by func is launched.

CUresult cuParamSetSize(CUfunction func, unsigned int numbytes);

sets through numbytes the total size in bytes needed by the function parameters of function func.

CUresult cuParamSeti(CUfunction func, unsigned int offset, unsigned int value);

sets an integer parameter that will be specified the next time the kernel corresponding to func will be invoked. offset is a byte offset.

CUresult cuParamSetf(CUfunction func, unsigned int offset, float value);

sets a floating point parameter that will be specified the next time the kernel corresponding to func will be invoked. offset is a byte offset.

CUresult cuParamSetv(CUfunction func, unsigned int offset, void* ptr, unsigned int numbytes);

copies an arbitrary amount of data into the parameter space of the kernel corresponding to func. offset is a byte offset.

CUresult cuParamSetArray(CUfunction func, unsigned int texunit, CUarray array);

makes the array array available to a device program as a texture. offset gives the offset of the sampler that the array is to be bound to. For texture references whose handles were passed back by cuModuleGetTexRef(), the special value CU_PARAM_TR_DEFAULT directs the driver to infer this value from the module.

CUresult cuLaunch(CUfunction func);

invokes the kernel func on a 1×1 grid of blocks. The block contains the number of threads specified by a previous call to cuFuncSetBlockShape().

CUresult cuLaunchGrid(CUfunction func, unsigned int grid_width, unsigned int grid_height);

invokes the kernel on a grid_width x grid_height grid of blocks. Each block contains the number of threads specified by a previous call to cuFuncSetBlockShape().

4.5.3.8 OpenGL Interoperability

CUresult cuGLInit(void);

initializes OpenGL interoperability. It must be called before performing any other OpenGL interoperability operations. It may fail if the needed OpenGL driver facilities are not available.

CUresult cuGLRegisterBufferObject(GLuint bufferObj);

registers the buffer object of ID bufferObj for access by CUDA. This function must be called before CUDA can map the buffer object. While it is registered, the buffer object cannot be used by any OpenGL commands except as a data source for OpenGL drawing commands.

CUresult cuGLMapBufferObject(CUdeviceptr* devPtr, unsigned int* size, GLuint bufferObj);
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maps the buffer object of ID `bufferObj` into the address space of the current CUDA context and returns in `*devPtr` and `*size` the base pointer and size of the resulting mapping.

```c
CUresult cuGLUnmapBufferObject(GLuint bufferObj);
```

unmaps the buffer object of ID `bufferObj` for access by CUDA.

```c
CUresult cuGLUnregisterBufferObject(GLuint bufferObj);
```

unregisters the buffer object of ID `bufferObj` for access by CUDA.

4.5.3.9 Direct3D Interoperability

```c
CUresult cuD3D9Begin(IDirect3DDevice9* device);
```

initializes interoperability with the Direct3D device `device`. This function must be called before CUDA can map any objects from `device`. The application can then map vertex buffers owned by the Direct3D device until `cuD3D9End()` is called.

```c
CUresult cuD3D9End();
```

concludes interoperability with the Direct3D device previously specified to `cuD3D9Begin()`.

```c
CUresult cuD3D9RegisterVertexBuffer(IDirect3DVertexBuffer9* VB);
```

registers the Direct3D vertex buffer `VB` for access by CUDA.

```c
CUresult cuD3D9MapVertexBuffer(CUdeviceptr* devPtr,
                               unsigned int* size,
                               IDirect3DVertexBuffer9* VB);
```

maps the Direct3D vertex buffer `VB` into the address space of the current CUDA context and returns in `*devPtr` and `*size` the base pointer and size of the resulting mapping.

```c
CUresult cuD3D9UnmapVertexBuffer(IDirect3DVertexBuffer9* VB);
```

unmaps the vertex buffer `VB` for access by CUDA.
5.1 General Specification

The GeForce 8800 Series has the following characteristics:

- The maximum number of threads per block is 512;
- The maximum size of each dimension of a grid of thread blocks is 65535;
- The number of multiprocessors is
  - 16 at 675 MHz for the GeForce 8800 GTX,
  - 12 at 600 MHz for the GeForce 8800 GTS;
- The amount of device memory is
  - 768 MB for the GeForce 8800 GTX,
  - 640 MB for the GeForce 8800 GTS;
- The amount of shared memory available per multiprocessor is 16 KB divided into 16 banks (see Section 6.1.2.4);
- The amount of constant memory available is 64 KB with a cache working set of 8 KB per multiprocessor;
- The cache working set for 1D textures is 8 KB per multiprocessor;
- The warp size is 32 threads;
- Texture filtering weights are stored in 9-bit fixed point format with 8 bits of fractional value.
- In Beta version 0.8, the maximum observed bandwidth between system memory and device memory is 2 GB/s.

Each multiprocessor is composed of eight processors running at twice the clock frequencies mentioned above, so that a multiprocessor is able to process the 32 threads of a warp in two clock cycles.
5.2 Floating-Point Standard

The GeForce 8800 Series follows the IEEE-754 standard for single-precision binary floating-point arithmetic with the following deviations:

- Addition and multiplication are often combined into a single multiply-add instruction (FMAD);
- Division is implemented via the reciprocal in a non-standard-compliant way;
- Square root is implemented via the reciprocal square root in a non-standard-compliant way;
- For addition and multiplication, only round-to-nearest-even and round-towards-zero are supported via static rounding modes; directed rounding towards +/- infinity is not supported;
- There is no dynamically configurable rounding mode;
- Denormalized source operands are treated as zero;
- Underflowed results are flushed to zero;
- There is no mechanism for detecting that a floating-point exception has occurred and floating-point exceptions are always masked, but when an exception occurs the masked response is standard compliant;
- Signaling NaNs are not supported.
- The result of an operation involving one or more input NaNs is not one of the input NaNs, but a canonical NaN of bit pattern 0x7fffffff. Note that in accordance to the IEEE-754R standard, if one of the input parameters to min() or max() is NaN, but not the other, the result is the non-NaN parameter.

The conversion of a floating-point value to an integer value in the case where the floating-point value falls outside the range of the integer format is left undefined by IEEE-754. For the GeForce 8800 Series, the behavior is to clamp to the end of the supported range. This is unlike the x86 architecture behaves.
6.1 Instruction Performance

To process an instruction for a warp of threads, a multiprocessor must:

- Read the instruction operands for each thread of the warp,
- Execute the instruction,
- Write the result for each thread of the warp.

Therefore, the effective instruction throughput depends on the nominal instruction throughput as well as the memory latency and bandwidth. It is maximized by:

- Minimizing the use of instructions with low throughput (see Section 6.1.1),
- Maximizing the use of the available memory bandwidth for each category of memory (see Section 6.1.2),
- Allowing the thread scheduler to overlap memory transactions with mathematical computations as much as possible, which requires that:
  - The program executed by the threads is of high arithmetic intensity, that is, has a high number of arithmetic operations per memory operation;
  - There are many threads that can be run concurrently as detailed in Section 6.1.2.

6.1.1 Instruction Throughput

6.1.1.1 Arithmetic Instructions

To issue one instruction for a warp, a multiprocessor takes:

- 2 clock cycles for floating-point add, floating-point multiply, floating-point multiply-add, integer add, bitwise operations, compare, min, max, type conversion instruction;
- 8 clock cycles for reciprocal, reciprocal square root, \( \log(x) \) (see Table A-2).

32-bit integer multiplication takes 8 clock cycles, but \_mul24 and \_umul24 (see Appendix A) provide signed and unsigned 24-bit integer multiplication in 2 clock cycles. Integer division and modulo operation are particularly costly and should be avoided if possible or replaced with bitwise operations whenever possible: If \( n \) is a
power of 2, \((i/n)\) is equivalent to \((i >> \log_2(n))\) and \((i \&\ n)\) is equivalent to \((i \& (n-1))\); the compiler will perform these conversions if \(n\) is literal.

Other functions take more clock cycles as they are implemented as combinations of several instructions.

Floating-point square root is implemented as a reciprocal square root followed by a reciprocal, so it takes 16 clock cycles for a warp.

Floating-point division takes 18 clock cycles, but \(_{\text{fdividef}}(x, y)\) provides a faster version at 10 clock cycles (see Appendix A).

\(_{\text{sin}}(x), _{\text{cos}}(x), _{\text{exp}}(x)\) take 16 clock cycles.

Sometimes, the compiler must insert conversion instructions, introducing additional execution cycles. This is the case for:

- Functions operating on \textbf{char} or \textbf{short} whose operands generally need to be converted to \textbf{int},
- Double-precision floating-point constants (defined without any type suffix) used as input to single-precision floating-point computations,
- Single-precision floating-point variables used as input parameters to the double-precision version of the mathematical functions defined in Table A-1.

The two last cases can be avoided by using:

- Single-precision floating-point constants, defined with an \textbf{f} suffix such as \(3.141592653589793f, 1.0f, 0.5f\),
- The single-precision version of the mathematical functions, defined with an \textbf{f} suffix as well, such as \textbf{sinf()}, \textbf{logf()}, \textbf{expf}().

For single precision code, we highly recommend use of the single precision math functions. When compiling for devices without native double precision support, the double precision math functions are by default mapped to their single precision equivalents. However, on those future devices that will support double precision, these functions will map to double precision implementations.

### 6.1.1.2 Control Flow Instructions

Any flow control instruction (\textbf{if}, \textbf{switch}, \textbf{do}, \textbf{for}, \textbf{while}) can significantly impact the effective instruction throughput by causing threads of the same warp to diverge, that is, to follow different execution paths. If this happens, the different executions paths have to be serialized, increasing the total number of instructions executed for this warp.

To obtain best performance in cases where the control flow depends on the thread ID, the controlling condition should be written so as to minimize the number of divergent warps. This is possible because the distribution of the warps across the block is deterministic as mentioned in Section 3.2. A trivial example is when the controlling condition only depends on \((\text{threadIdx} \div WSIZE)\) where \(WSIZE\) is the warp size. In this case, no warp diverges since the controlling condition is perfectly aligned with the warps.

Sometimes, the compiler may unroll loops or may optimize out \textbf{if} or \textbf{switch} statements by using branch predication instead, as detailed below. In these cases, no warp can ever diverge.
When using branch predication none of the instructions whose execution depends on the controlling condition gets skipped. Instead, each of them is associated with a per-thread condition code or *predicate* that is set to true or false based on the controlling condition and although each of these instructions gets scheduled for execution, only the instructions with a true predicate are actually executed. Instructions with a false predicate do not write results, and also do not evaluate addresses or read operands.

The compiler replaces a branch instruction with predicated instructions only if the number of instructions controlled by the branch condition is less or equal to a certain threshold: If the compiler determines that the condition is likely to produce many divergent warps, this threshold is 7, otherwise it is 4.

### 6.1.1.3 Memory Instructions

Memory instructions include any instruction that reads from or writes to shared or global memory. A multiprocessor takes 2 clock cycles to issue one memory instruction for a warp. When accessing global memory, there are, in addition, 200 to 300 clock cycles of memory latency.

As an example, the assignment operator in the following sample code:

```c
__shared__ float shared[32];
__device__ float device[32];
shared[threadIdx.x] = device[threadIdx.x];
```

takes 2 clock cycles to issue a read from global memory, 2 clock cycles to issue a write to shared memory, but above all 200 to 300 clock cycles to read a float from global memory.

Much of this global memory latency can be hidden by the thread scheduler if there are sufficient independent arithmetic instructions that can be issued while waiting for the global memory access to complete.

### 6.1.1.4 Synchronization Instruction

`__syncthreads__` takes 2 clock cycles to issue for a warp if no thread has to wait for any other threads.

### 6.1.2 Memory Bandwidth

The effective bandwidth of each memory space depends significantly on the memory access pattern as detailed in the following sub-sections.

Since device memory is of much higher latency and lower bandwidth than on-chip memory, device memory accesses should be minimized. A typical programming pattern is to stage data coming from device memory into shared memory; in other words, to have each thread of a block:

- Load data from device memory to shared memory,
- Synchronize with all the other threads of the block so that each thread can safely read shared memory locations that were written by different threads,
- Process the data in shared memory,
- Synchronize again if necessary to make sure that shared memory has been updated with the results,
- Write the results back to device memory.
6.1.2.1 Global Memory

The global memory space is not cached, so it is all the more important to follow the right access pattern to get maximum memory bandwidth, especially given how costly accesses to device memory are.

First, the device is capable of reading 64-bit or 128-bit words from global memory into registers in a single instruction. To have assignments such as:

\[
\text{__device\_type device[32];}
\]

\[
\text{type data = device[tid];}
\]

compile to a single load instruction, \text{type} must be such that \text{sizeof(type)} is equal to 4, 8, or 16 and variables of type \text{type} must be aligned to 4, 8, or 16 bytes (that is, have the 4, 8, or 16 least significant bits of their address equal to zero).

The alignment requirement is automatically fulfilled for built-in types of Section 4.3.1.1 like \text{float2} or \text{float4}.

For structures, the size and alignment requirements can be enforced by the compiler using the alignment specifiers \text{__align\_{8}} or \text{__align\_{16}}, such as

\[
\text{struct __align\_{8}}\{ \\
\text{  float a;}
\text{  float b;}
\}\;
\]

or

\[
\text{struct __align\_{16}}\{ \\
\text{  float a;}
\text{  float b;}
\text{  float c;}
\text{  float d;}
\}\;
\]

For structures larger than 16 bytes, the compiler generates several load instructions. To ensure that it generates the minimum number of instructions, such structures should be defined with \text{__align\_{16}}, such as

\[
\text{struct __align\_{16}}\{ \\
\text{  float a;}
\text{  float b;}
\text{  float c;}
\text{  float d;}
\text{  float e;}
\}\;
\]

which is compiled into two 128-bit load instructions instead of five 32-bit load instructions.

Second, the read and write addresses of each warp should be arranged so that the simultaneous memory accesses of the entire wrap can be coalesced into a single contiguous, aligned memory access.

It means that in each warp, thread number \text{N} within the warp should access address

\[
\text{WarpBaseAddress + N}
\]

where \text{WarpBaseAddress} is of type \text{type\_t} and \text{type} is such that it meets the size and alignment requirements discussed above.

Moreover, in the case of the GeForce 8800 Series:
WarpBaseAddress should be aligned to $16 \times \text{sizeof}(\text{type})$ bytes; in other words, it should have its $\log_2(16 \times \text{sizeof}(\text{type}))$ least significant bits equal to zero. Any address BaseAddress of a variable residing in global memory or returned by one of the memory allocation routines from Section 4.5.2.2 is always aligned to at least 256 bytes, so to satisfy the memory alignment constraint, WarpBaseAddress - BaseAddress should be a multiple of $16 \times \text{sizeof}(\text{type})$.

Memory accesses from threads belonging to the first half of a warp cannot be coalesced with memory accesses from threads belonging to the second half of the warp.

Note that if a warp fulfills all the requirements above, the per-thread memory accesses are coalesced even if some threads of the warp do not actually access memory.

A common global memory access pattern is when each thread of index $(tx, ty)$ accesses one element of a 2D array located at address BaseAddress of type type* and of width width using the following address:

$$\text{BaseAddress} + \text{width} \times ty + tx$$

In such a case, one gets memory coalescing for all warps of the thread block only if:

- The width of the thread block is a multiple of half the warp size;
- width is a multiple of 16.

In particular, this means that an array whose width is not a multiple of 16 will be accessed much more efficiently if it is actually allocated with a width rounded up to the closest multiple of 16 and its rows padded accordingly.

The cuMemAlloc2D() and cudaMalloc2D() functions and associated memory copy functions described in Sections 4.5.2.2 and 4.5.3.5 enable developers to write non-hardware-dependent code to allocate arrays that conform to these constraints.

### 6.1.2.2 Constant Memory

The constant memory space is cached so a read from constant memory costs one memory read from device memory only on a cache miss, otherwise it just costs one read from the constant cache.

For all threads of a warp, reading from the constant cache is as fast as reading from a register as long as all threads read the same address. The cost scales linearly with the number of different addresses read by all threads.

In the case of the GeForce 8800 Series, two threads can read two different addresses without additional cost if one belongs to the first half of the warp and the other belongs to the second half of the warp.

### 6.1.2.3 Texture Memory

The texture memory space is cached so a texture sampling costs one memory read from device memory only on a cache miss, otherwise it just costs one read from the texture cache. Texture filtering calculations are performed for every read by the texture unit.

The texture cache is optimized for 2D spatial locality, so threads of the same warp that read texture addresses that are close together will achieve best performance.
6.1.2.4 Shared Memory

Because it is on-chip, the shared memory space is much faster than the local and
global memory spaces. In fact, for all threads of a warp, accessing the shared
memory is as fast as accessing a register as long as there are no bank conflicts
between the threads, as detailed below.

To achieve high memory bandwidth, the shared memory space is divided into
equally-sized memory modules, called banks, which can be accessed simultaneously.
So, any memory read or write request made of \( n \) addresses that fall in \( n \) distinct
memory banks can be serviced in one clock cycle, yielding an effective bandwidth
that is \( n \) times as high as the bandwidth of a single module.

However, if two addresses of a memory request fall in the same memory bank, there
is a bank conflict and the access has to be serialized. The hardware splits a memory
request with bank conflicts into as many separate conflict-free requests as necessary,
decreasing the effective bandwidth by a factor equal to the number of separate
memory requests. If the number of separate memory requests is \( n \), the initial
memory request is said to cause \( n \)-way bank conflicts.

To get maximum performance, it is therefore important to understand how memory
addresses map to memory banks in order to schedule the memory requests so as to
minimize bank conflicts.

In the case of the shared memory space, the banks are organized such that
successive 32-bit words are assigned to successive banks and each bank has a
bandwidth of 32 bits per clock cycle.

For the GeForce 8800 Series, the warp size is 32 and the number of banks is 16 (see
Section 5.1). Therefore, a shared memory request requires two clock cycles for a
warp: One cycle to service the first half of the warp and one cycle to service the
second half of the same warp. As a consequence, there can be no bank conflict
between a thread belonging to the first half of a warp and a thread belonging to the
second half of the same warp.

A common case is for each thread to access a 32-bit word from an array indexed by
the thread ID \( \text{tid} \) and with some stride \( s \):

\[
\begin{align*}
\text{__shared__ float shared[32];} \\
\text{float data = shared[BaseIndex + s * tid];}
\end{align*}
\]

In this case, the threads \( \text{tid} \) and \( \text{tid+n} \) access the same bank whenever \( s*n \) is a
multiple of the number of banks \( m \) or equivalently, whenever \( n \) is a multiple of \( m/d \)
where \( d \) is the greatest common divisor of \( m \) and \( s \). As a consequence, there will be
no bank conflict only if the warp size, or for the GeForce 8800 Series, half the warp
size, is less than or equal to \( m/d \). For the GeForce 8800 Series, this translates to no
bank conflict only if \( d \) is equal to 1, or in other words, only if \( s \) is odd since \( m \) is a
power of two.

Other cases worth mentioning are when each thread accesses an element that is
smaller or larger than 32 bits in size. For example, there will be bank conflicts if an
array of \text{char} is accessed the following way:

\[
\begin{align*}
\text{__shared__ char shared[32];} \\
\text{char data = shared[BaseIndex + tid];}
\end{align*}
\]
because `shared[0], shared[1], shared[2],` and `shared[3],` for example, belong to the same bank. There will not be any bank conflict however, if the same array is accessed the following way:

```c
char data = shared[BaseIndex + 4 * tid];
```

A structure assignment is compiled into as many memory requests as there are members in the structure, so the following code, for example:

```c
__shared__ struct type shared[32];
struct type data = shared[BaseIndex + tid];
```

results in:

- Three separate memory reads without bank conflicts if `type` is defined as
  ```c
  struct type {
    float x, y, z;
  };
  ```
  since each member is accessed with a stride of three 32-bit words;

- Two separate memory reads with bank conflicts if `type` is defined as
  ```c
  struct type {
    float x, y;
  };
  ```
  since each member is accessed with a stride of two 32-bit words;

- Two separate memory reads with bank conflicts if `type` is defined as
  ```c
  struct type {
    float f;
    char c;
  };
  ```
  since each member is accessed with a stride of five bytes.

Finally, the shared memory space also features a broadcast mechanism whereby a 32-bit word can be read and broadcast to several threads in one clock cycle. This reduces the number of bank conflicts when several threads of a warp read from an address within the same 32-bit word. More precisely, a memory read request made of several addresses is serviced in several clock cycles by servicing one conflict-free subset of these addresses per clock cycle until all addresses have been serviced; the subset is built at every clock cycle from the remaining addresses that have yet to be serviced using the following procedure:

- Select one of the words pointed to by the remaining addresses as the broadcast word,
- Include in the subset:
  - All addresses that are within the broadcast word,
  - One address for each bank pointed to by the remaining addresses.

Which word is selected as the broadcast word and which address is picked up for each bank at each cycle are unspecified.

A common conflict-free case is when all threads of a warp read from an address within the same 32-bit word.
Chapter 6. Performance Guidelines

Figure 6-1 and Figure 6-2 show some examples of conflict-free memory accesses while Figure 6-3 and Figure 6-4 show some examples of memory accesses that cause bank conflicts.
Figure 6-1. Examples of Shared Memory Access Patterns without Bank Conflicts
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Figure 6-2. Examples of Shared Memory Access Patterns without Bank Conflicts

Left: linear addressing with a stride of three 32-bit words. Right: all threads read from an address within the same 32-bit word.
Left: linear addressing with a stride of two 32-bit words causes 2-way bank conflicts. Right: linear addressing with a stride of eight 32-bit words causes 8-way bank conflicts.

Figure 6-3. Examples of Shared Memory Access Patterns with Bank Conflicts
This access pattern causes either no bank conflicts if the word from bank 5 is chosen as the broadcast word during the first clock cycle or 2-way bank conflicts if it is chosen as the broadcast word during the second clock cycle.

**Figure 6-4. Example of Shared Memory Access Pattern with or without Bank Conflicts**
Chapter 6. Performance Guidelines

6.1.2.5 Registers

Generally, accessing a register is zero extra clock cycles per instruction, but delays may occur due to register read-after-write dependencies and register memory bank conflicts.

The delays introduced by read-after-write dependencies can be ignored as soon as there are at least 192 concurrent threads per multiprocessor to hide them.

The compiler and thread scheduler schedule the instructions as optimally as possible to avoid register memory bank conflicts; the application has no control over these. In particular, there is no need to pack data into float4 or int4 types.

6.2 Number of Threads per Block

Given a total number of threads per grid, the number of threads per block, or equivalently the number of blocks, should be chosen to maximize the utilization of the available computing resources. This means that there should be at least as many blocks as there are multiprocessors in the device.

Furthermore, running only one block per multiprocessor will force the multiprocessor to idle during thread synchronization and also during device memory reads if there are not enough threads per block to cover the load latency. It is therefore better to allow for two or more blocks to run concurrently on each multiprocessor to allow overlap between blocks that wait and blocks that can run. For this to happen, not only should there be at least twice as many blocks as there are multiprocessors in the device, but also the amount of allocated shared memory per block should be at most half the total amount of shared memory available per multiprocessor. More thread blocks stream in pipeline fashion through the device and amortize overhead even more.

With a high enough number of blocks, the number of threads per block should be chosen as a multiple of the warp size to avoid wasting computing resources with under-populated warps. Allocating more threads per block is better for efficient time slicing, but the more threads per block, the fewer registers are available per thread. This might prevent a kernel invocation from succeeding if the kernel compiles to more registers than are allowed by the execution configuration.

For the GeForce 8800 Series, 64 threads per block is minimal and makes sense only if there are multiple concurrent blocks. 192 or 256 threads per block is better and usually allows for enough registers to compile.

The number of blocks per grid should be at least 100 if one wants it to scale to future devices; 1000 blocks will scale across several generations.

6.3 Data Transfer between Host and Device

The bandwidth between the device and the device memory is much higher than the bandwidth between the device memory and the host memory. Therefore, one should strive to minimize data transfer between the host and the device. For example, intermediate data structures may be created in device memory, operated on
by the device, and destroyed without ever being mapped by the host or copied to host memory.

Also, because of the overhead associated with each transfer, batching many small transfers into a big one always performs much better than making each transfer separately.
Chapter 7.
Example of Matrix Multiplication

7.1 Overview

The task of computing the product $C$ of two matrices $A$ and $B$ of dimensions $(w_A, h_A)$ and $(w_B, w_A)$ respectively, is split among several threads in the following way:

- Each thread block is responsible for computing one square sub-matrix $C_{sub}$ of $C$;
- Each thread within the block is responsible for computing one element of $C_{sub}$.

The dimension $block\_size$ of $C_{sub}$ is chosen equal to 16, so that the number of threads per block is a multiple of the warp size (Section 6.2) and remains below the maximum number of threads per block (Section 5.1).

As illustrated in Figure 7-1, $C_{sub}$ is equal to the product of two rectangular matrices: the sub-matrix of $A$ of dimension $(w_A, block\_size)$ that has the same line indices as $C_{sub}$ and the sub-matrix of $B$ of dimension $(block\_size, w_A)$ that has the same column indices as $C_{sub}$. In order to fit into the device’s resources, these two rectangular matrices are divided into as many square matrices of dimension $block\_size$ as necessary and $C_{sub}$ is computed as the sum of the products of these square matrices. Each of these products is performed by first loading the two corresponding square matrices from global memory to shared memory with one thread loading one element of each matrix, and then by having each thread compute one element of the product. Each thread accumulates the result of each of these products into a register and once done writes the result to global memory.

By blocking the computation this way, we take advantage of fast shared memory and save a lot of global memory bandwidth since $A$ and $B$ are read from global memory only $(w_A / block\_size)$ times.
Each thread block computes one sub-matrix \( C_{sub} \) of \( C \). Each thread within the block computes one element of \( C_{sub} \).

Figure 7-1. Matrix Multiplication
7.2 Source Code Listing

```
// Thread block size
#define BLOCK_SIZE 16

// Forward declaration
// of the device multiplication function
__global__ void Muld(float*, float*,
                   int, int,
                   float*);

// Host multiplication function
// Compute C = A * B
// hA is the height of A
// wA is the width of A
// wB is the width of B
void Mul(const float* A, const float* B,
         int hA, int wA, int wB,
         float* C)
{
  int size;

  // Load A and B to the device
  float* Ad;
  size = hA * wA * sizeof(float);
  cudaMalloc((void**)&Ad, size);
  cudaMemcpy(Ad, A, size, cudaMemcpyHostToDevice);
  float* Bd;
  size = wA * wB * sizeof(float);
  cudaMalloc((void**)&Bd, size);
  cudaMemcpy(Bd, B, size, cudaMemcpyHostToDevice);

  // Allocate C on the device
  float* Cd;
  size = hA * wB * sizeof(float);
  cudaMalloc((void**)&Cd, size);

  // Compute the execution configuration
  dim3 dimBlock(BLOCK_SIZE, BLOCK_SIZE);
  dim3 dimGrid(wB / dimBlock.x, hA / dimBlock.y);

  // Launch the device computation
  Muld<<<dimGrid, dimBlock>>>(Ad, Bd, wA, wB, Cd);

  // Read C from the device
  cudaMemcpy(C, Cd, size, cudaMemcpyDeviceToHost);

  // Free device memory
  cudaFree(Ad);
  cudaFree(Bd);
  cudaFree(Cd);
}
```
// Device multiplication function called by Mul()
// Compute C = A * B
// wA is the width of A
// wB is the width of B
__global__ void Muld(float* A, float* B,
    int wA, int wB,
    float* C)
{
    // Block index
    int bx = blockIdx.x;
    int by = blockIdx.y;

    // Thread index
    int tx = threadIdx.x;
    int ty = threadIdx.y;

    // Index of the first sub-matrix of A processed
    // by the block
    int aBegin = wA * BLOCK_SIZE * by;

    // Index of the last sub-matrix of A processed
    // by the block
    int aEnd = aBegin + wA;

    // Step size used to iterate through
    // the sub-matrices of A
    int aStep = BLOCK_SIZE;

    // Index of the first sub-matrix of B processed
    // by the block
    int bBegin = BLOCK_SIZE * bx;

    // Step size used to iterate through
    // the sub-matrices of B
    int bStep = BLOCK_SIZE * wB;

    // The element of the block sub-matrix
    // that is computed by the thread
    float Csub = 0;

    // Loop over all the sub-matrices of A and B
    // required to compute the block sub-matrix
    for (int a = aBegin, b = bBegin;
        a < aEnd;
        a += aStep, b += bStep) {

        // Shared memory for the sub-matrix of A
        __shared__ float As[BLOCK_SIZE][BLOCK_SIZE];

        // Shared memory for the sub-matrix of B
        __shared__ float Bs[BLOCK_SIZE][BLOCK_SIZE];

        // Load the matrices from global memory
        // to shared memory; each thread loads
        // one element of each matrix
        As[ty][tx] = A[a + wA * ty + tx];
        Bs[ty][tx] = B[b + wB * ty + tx];
    }
}
7.3 Source Code Walkthrough

The source code contains two functions:

- **Mul()**, a host function serving as a wrapper to Muld();
- **Muld()**, a kernel that executes the matrix multiplication on the device.

### 7.3.1 Mul()

**Mul()** takes as input:
- Two pointers to host memory that point to the elements of A and B,
- The height and width of A and the width of B,
- A pointer to host memory that points where C should be written.

**Mul()** performs the following operations:
- It allocates enough global memory to store A, B, and C using `cudaMalloc()`;
- It copies A and B from host memory to global memory using `cudaMemcpy()`;
- It calls **Muld()** to compute C on the device;
- It copies C from global memory to host memory using `cudaMemcpy()`;
- It frees the global memory allocated for A, B, and C using `cudaFree()`.

### 7.3.2 Muld()

**Muld()** has the same input as **Mul()**, except that pointers point to device memory instead of host memory.

For each block, **Muld()** iterates through all the sub-matrices of A and B required to compute C$_{sub}$. At each iteration:

```c
__syncthreads();

// Multiply the two matrices together;
// each thread computes one element
// of the block sub-matrix
for (int k = 0; k < BLOCK_SIZE; ++k)
    Csub += As[ty][k] * Bs[k][tx];

__syncthreads();

// Write the block sub-matrix to global memory;
// each thread writes one element
int c = wB * BLOCK_SIZE * by + BLOCK_SIZE * bx;
C[c + wB * ty + tx] = Csub;
```
Example of Matrix Multiplication

- It loads one sub-matrix of $A$ and one sub-matrix of $B$ from global memory to shared memory;
- It synchronizes to make sure that both sub-matrices are fully loaded by all the threads within the block;
- It computes the product of the two sub-matrices and adds it to the product obtained during the previous iteration;
- It synchronizes again to make sure that the product of the two sub-matrices is done before starting the next iteration.

Once all sub-matrices have been handled, $C_{sub}$ is fully computed and $\text{Muld()}$ writes it to global memory.

$\text{Muld()}$ is written to maximize memory performance according to Section 6.1.2.1 and 6.1.2.4.

Indeed, assuming that $wA$ and $wB$ are multiples of 16 as suggested in Section 6.1.2.1, global memory coalescing is ensured because $a, b, c$ are all multiples of $\text{BLOCK}_\text{SIZE}$, which is equal to 16.

There is also no shared memory bank conflict since for each half of a warp, $ty$ and $k$ are the same for all threads and $tx$ varies from 0 to 15, so each thread accesses a different bank for the memory accesses $A[ty][tx], B[ty][tx]$, and $B[k][tx]$ and the same bank for the memory access $A[ty][k]$. 
Table A-1 below lists all the mathematical standard library functions supported by the CUDA runtime library. It also specifies the error bounds of each function when executed on the device and on the host, in case the host does no supply the function. These bounds are generated from extensive but not exhaustive tests, so these are not guaranteed bounds. For every function `func()`, the CUDA runtime also supports its single-precision counterpart `funcf()` when applicable, with the same error bounds.

Addition and multiplication are IEEE-compliant, so have a maximum error of 0.5 ulp. They are however often combined into a single multiply-add instruction (FMAD), which truncates the intermediate result of the multiplication.

The recommended way to round a floating-point operand to an integer, with the result being a floating-point number is `rintf()`, not `roundf()`. The reason is that `roundf()` maps to an 8-instruction sequence, whereas `rintf()` maps to a single instruction.

`truncf()`, `ceilf()`, and `floorf()` each map to a single instruction as well.

Table A-1. Mathematical Standard Library Functions with Maximum ULP Error

<table>
<thead>
<tr>
<th>Function</th>
<th>Maximum ulp error</th>
</tr>
</thead>
<tbody>
<tr>
<td>x/y</td>
<td>2 (full range)</td>
</tr>
<tr>
<td>1/x</td>
<td>1 (full range)</td>
</tr>
<tr>
<td>1/sqrt(x)</td>
<td>2 (full range)</td>
</tr>
<tr>
<td>sqrt(x)</td>
<td>3 (full range)</td>
</tr>
<tr>
<td>cbrt(x)</td>
<td>1 (full range)</td>
</tr>
<tr>
<td>hypot(x)</td>
<td>3 (full range)</td>
</tr>
<tr>
<td>exp(x)</td>
<td>2 (full range)</td>
</tr>
<tr>
<td>exp2(x)</td>
<td>2 (full range)</td>
</tr>
<tr>
<td>expm1(x)</td>
<td>4 (full range)</td>
</tr>
<tr>
<td>log(x)</td>
<td>3 (full range)</td>
</tr>
<tr>
<td>log2(x)</td>
<td>4 (full range)</td>
</tr>
<tr>
<td>log10(x)</td>
<td>4 (full range)</td>
</tr>
</tbody>
</table>
### Appendix A. Mathematics Functions

<table>
<thead>
<tr>
<th>Function</th>
<th>Maximum ulp error</th>
</tr>
</thead>
<tbody>
<tr>
<td>log1p(x)</td>
<td>4 (full range)</td>
</tr>
<tr>
<td>sin(x)</td>
<td>2 (inside interval -12988 ... +12988; larger outside)</td>
</tr>
<tr>
<td>cos(x)</td>
<td>3 (inside interval -12988 ... +12988; larger outside)</td>
</tr>
<tr>
<td>tan(x)</td>
<td>4 (inside interval -12988 ... +12988; larger outside)</td>
</tr>
<tr>
<td>asin(x)</td>
<td>4 (full range)</td>
</tr>
<tr>
<td>acos(x)</td>
<td>3 (full range)</td>
</tr>
<tr>
<td>atan(x)</td>
<td>2 (full range)</td>
</tr>
<tr>
<td>atan2(y, x)</td>
<td>3 (full range)</td>
</tr>
<tr>
<td>sinh(x)</td>
<td>3 (full range)</td>
</tr>
<tr>
<td>cosh(x)</td>
<td>2 (full range)</td>
</tr>
<tr>
<td>tanh(x)</td>
<td>2 (full range)</td>
</tr>
<tr>
<td>asinh(x)</td>
<td>3 (full range)</td>
</tr>
<tr>
<td>acosh(x)</td>
<td>5 (full range)</td>
</tr>
<tr>
<td>atanh(x)</td>
<td>4 (full range)</td>
</tr>
<tr>
<td>pow(x, y)</td>
<td>16 (for x outside interval 0.75 ... 1.195; larger for x inside)</td>
</tr>
<tr>
<td>erf(x)</td>
<td>4 (full range)</td>
</tr>
<tr>
<td>erfc(x)</td>
<td>8 (full range)</td>
</tr>
<tr>
<td>lgamma(x)</td>
<td>6 (outside interval -11 ... -2.166; larger inside)</td>
</tr>
<tr>
<td>frexp(x, exp)</td>
<td>0 (full range)</td>
</tr>
<tr>
<td>ldexp(x, exp)</td>
<td>0 (full range)</td>
</tr>
<tr>
<td>scalbn(x, n)</td>
<td>0 (full range)</td>
</tr>
<tr>
<td>logb(x)</td>
<td>0 (full range)</td>
</tr>
<tr>
<td>ilogb(x)</td>
<td>0 (full range)</td>
</tr>
<tr>
<td>fmod(x, y)</td>
<td>0 (full range)</td>
</tr>
<tr>
<td>modf(x, iptr)</td>
<td>0 (full range)</td>
</tr>
<tr>
<td>fdim(x, y)</td>
<td>0 (full range)</td>
</tr>
<tr>
<td>trunc(x)</td>
<td>0 (full range)</td>
</tr>
<tr>
<td>round(x)</td>
<td>0 (full range)</td>
</tr>
<tr>
<td>rint(x)</td>
<td>0 (full range)</td>
</tr>
<tr>
<td>nearbyint(x)</td>
<td>0 (full range)</td>
</tr>
<tr>
<td>ceil(x)</td>
<td>0 (full range)</td>
</tr>
<tr>
<td>floor(x)</td>
<td>0 (full range)</td>
</tr>
<tr>
<td>signbit(x)</td>
<td>N/A</td>
</tr>
<tr>
<td>isnf(x)</td>
<td>N/A</td>
</tr>
<tr>
<td>isnan(x)</td>
<td>N/A</td>
</tr>
<tr>
<td>Isfinite(x)</td>
<td>N/A</td>
</tr>
<tr>
<td>Copysign(x, y)</td>
<td>N/A</td>
</tr>
<tr>
<td>Min(x, y)</td>
<td>N/A</td>
</tr>
<tr>
<td>Max(x, y)</td>
<td>N/A</td>
</tr>
<tr>
<td>abs(x)</td>
<td>N/A</td>
</tr>
</tbody>
</table>
For some of the functions of Table A-1, a less accurate, but faster version exists with the same name prefixed with \( \_\_ \) (such as \( \_\_\text{sin}(x) \)). These functions are listed in Table A-2. The error bounds for the functions prefixed with \( \_\_ \) are GPU-specific.

Both the regular floating-point division and \( \_\_\text{fdivide}(x, y) \) have same accuracy, but for \( 2^{126} < y < 2^{128}, \_\_\text{fdivide}(x, y) \) delivers a result of zero, whereas the regular division delivers the correct result to within the accuracy stated in Table A-1. Besides, for \( 2^{126} < y < 2^{128} \), if \( x \) is infinity, \( \_\_\text{fdivide}(x, y) \) delivers a NaN (as a result of multiplying infinity by zero), while the regular division returns infinity.

\( \_\_[u]\text{mul24}(x, y) \) computes the product of the 24 least significant bits of the integer parameters \( x \) and \( y \) and delivers the 32 least significant bits of the result. If any of the 8 most significant bits of either \( x \) or \( y \) are set, the result is undefined.

\( \_\_[u]\text{mulhi}(x, y) \) computes the product of the integer parameters \( x \) and \( y \) and delivers the 32 most significant bits of the 64-bit result.

### Table A-2. Fast Mathematical Functions Supported by the CUDA Runtime Library with Respective Error Bounds for the GeForce 8800 Series

<table>
<thead>
<tr>
<th>Function</th>
<th>Error bounds</th>
</tr>
</thead>
<tbody>
<tr>
<td>( __\text{fdivide}(x, y) )</td>
<td>For ( y ) in ([2^{-126}, 2^{128}]), the maximum ulp error is 2.</td>
</tr>
<tr>
<td>( __\text{exp}(x) )</td>
<td>The maximum ulp error is ( 2 + \text{floor}(\text{abs}(1.16 \times x)) ).</td>
</tr>
<tr>
<td>( __\text{log}(x) )</td>
<td>For ( x ) in ([0.5, 2]), the maximum absolute error is ( 2^{-21.41} ), otherwise, the maximum ulp error is 3.</td>
</tr>
<tr>
<td>( __\text{log2}(x) )</td>
<td>For ( x ) in ([0.5, 2]), the maximum absolute error is ( 2^{-22} ), otherwise, the maximum ulp error is 2.</td>
</tr>
<tr>
<td>( __\text{log10}(x) )</td>
<td>For ( x ) in ([0.5, 2]), the maximum absolute error is ( 2^{-24} ), otherwise, the maximum ulp error is 3.</td>
</tr>
<tr>
<td>( __\text{sin}(x) )</td>
<td>For ( x ) in ([-\pi, \pi]), the maximum absolute error is ( 2^{-21.41} ), and larger otherwise.</td>
</tr>
<tr>
<td>( __\text{cos}(x) )</td>
<td>For ( x ) in ([-\pi, \pi]), the maximum absolute error is ( 2^{-21.19} ), and larger otherwise.</td>
</tr>
<tr>
<td>( __\text{tan}(x) )</td>
<td>Derived from its implementation as ( __\text{sin}(x) \times 1 / __\text{cos}(x) ).</td>
</tr>
<tr>
<td>( __\text{pow}(x, y) )</td>
<td>Derived from its implementation as ( \exp(2(y \times __\text{log2}(x))) ).</td>
</tr>
<tr>
<td>( __\text{mul24}(x, y) )</td>
<td>N/A</td>
</tr>
<tr>
<td>( __\text{umul24}(x, y) )</td>
<td>N/A</td>
</tr>
<tr>
<td>( __\text{mulhi}(x, y) )</td>
<td>N/A</td>
</tr>
<tr>
<td>( __\text{umulhi}(x, y) )</td>
<td>N/A</td>
</tr>
<tr>
<td>( __\text{int_as_float}(x) )</td>
<td>N/A</td>
</tr>
<tr>
<td>( __\text{float_as_int}(x) )</td>
<td>N/A</td>
</tr>
<tr>
<td>( __\text{saturate}(x) )</td>
<td>N/A</td>
</tr>
</tbody>
</table>
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