Beyond Reuse Distance Analysis: Dynamic Analysis for Characterization of Data Locality Potential

Naznin Fauzia, Ohio State University
Venmugil Elango, Ohio State University
Mahesh Ravishankar, Ohio State University
Louis-Noël Pouchet, University of California Los Angeles
J. Ramanujam, Louisiana State University
Fabrice Rastello, INRIA COMPSYS / ENS Lyon
Atanas Rountev, Ohio State University
P. Sadayappan, Ohio State University

Emerging computer architectures will feature drastically decreased flops/byte (ratio of peak processing rate to memory bandwidth) as highlighted by recent studies on Exascale architectural trends. Further, flops are getting cheaper while the energy cost of data movement is increasingly dominant. The understanding and characterization of data locality properties of computations is critical in order to guide efforts to enhance data locality.

Reuse distance analysis of memory address traces is a valuable tool to perform data locality characterization of programs. A single reuse distance analysis can be used to estimate the number of cache misses in a fully associative LRU cache of any size, thereby providing lower bound estimates on the minimum bandwidth requirements at different levels of the memory hierarchy to avoid being bandwidth bound. However, such an analysis only holds for the particular execution order that produced the trace. It cannot estimate potential improvement in data locality through dependence preserving transformations that change the execution schedule of the operations in the computation.

In this article, we develop a novel dynamic analysis approach to characterize the inherent locality properties of a computation and thereby assess the potential for data locality enhancement via dependence preserving transformations. The execution trace of a code is analyzed to extract a computational directed acyclic graph (CDAG) of the data dependences. The CDAG is then partitioned into convex subsets, and the convex partitioning is used to reorder the operations in the execution trace to enhance data locality. The approach enables us to go beyond reuse distance analysis of a single specific order of execution of the operations of a computation in characterization of its data locality properties. It can serve a valuable role in identifying promising code regions for manual transformation, as well as assessing the effectiveness of compiler transformations for data locality enhancement. We demonstrate the effectiveness of the approach using a number of benchmarks, including case studies where the potential shown by the analysis is exploited to achieve lower data movement costs and better performance.

1. INTRODUCTION

Advances in technology over the last few decades have yielded significantly different rates of improvement in the computational performance of processors relative to the speed of memory access. The Intel 80286 processor introduced in 1982 had an operation execution latency of 320 ns and a main memory access time of 225 ns [Hennessy and Patterson 2011]. The recent Intel Core i7 processor has an operation latency of 4ns and a memory latency of 37 ns, illustrating an order of magnitude shift in the ratio of operation latency to memory access latency. Since processors use parallelism and pipelining in execution of operations and for memory access, it is instructive to also examine the trends in the peak execution throughput and memory bandwidth for these two processors: 2 MIPS and 13 MBytes/sec for the 80286 versus 50,000 MIPS and 16,000 MBytes/sec for the Core i7. The ratio of peak computational rate to peak memory access bandwidth has also changed by more than an order of magnitude.

Because of the significant mismatch between computational latency and throughput when compared to main memory latency and bandwidth, the use of hierarchical memory systems and the exploitation of significant data reuse in the higher (i.e., faster) levels of the memory hierarchy is critical for high performance. Techniques such as pre-fetching and overlap of computation with communication can be used to mitigate the impact of high memory access latency on performance, but the mismatch between maximum computational rate and peak memory bandwidth is much more fundamental; *the only solution is to limit the volume of data movement to/from memory by enhancing data reuse in registers and higher levels of the cache.*

A significant number of research efforts have focused on improving data locality, by developing new algorithms such as the so called *communication avoiding* algorithms [Demmel et al. 2012; Ballard et al. 2011a; 2011b] as well as automated compiler transformation techniques [Irigoin and Triolet 1988; Wolf and Lam 1991; Kennedy and McKinley 1993; Bondhugula et al. 2008]. With future systems, the cost of data movement through the memory hierarchy is expected to become even more dominant relative to the cost of performing arithmetic operations [Bergman et al. 2008; Fuller and Millett 2011; Shalf et al. 2011], both in terms of throughput and energy. Therefore optimizing data access costs will become ever more critical in the coming years. Given the crucial importance of optimizing data access costs in systems with hierarchical memory, it is of great interest to develop tools and techniques to assess the inherent data locality characteristics of different parts of a computation, and the potential for data locality enhancement via dependence preserving transformations.

Reuse distance (also called LRU stack distance) is a widely used approach to model data locality [Mattson et al. 1970; Ding and Zhong 2003] in computations. Since its introduction in 1970 by Mattson et al. [Mattson et al. 1970], reuse distance analysis has found numerous applications in performance analysis and optimization, such as cache miss rate prediction [Zhong et al. 2003; Marin and Mellor-Crummey 2004; Jiang et al. 2010], program phase detection [Shen et al. 2004], data layout optimization [Zhong et al. 2004], virtual memory management [Cascaval et al. 2005] and I/O performance optimization [Jiang and Zhang 2005]. Defined as the number of distinct memory references between two successive references to the same location, reuse distance provides a quantification of the locality present in a data reference trace. A key property of the reuse distance characterization of an address trace is that, for a fully associative cache of size S, every reference with reuse distance $d \leq S$ would be a hit and all others misses. Thus, a single reuse distance analysis of an address trace allows an estimation of the total number of hits/misses for an idealized cache of any size, from a cumulative reuse distance histogram. In contrast, cache simulation to determine the number of hits/misses would have to be repeated for each cache size of interest. Although real caches have non-unit line size and finite associativity, the data transfer volume estimated from the number of cache misses via reuse distance analysis can serve as a valuable lower bound estimate for any real cache.

Although reuse distance analysis has found many uses in characterizing data locality in computations, it has a fundamental constraint: *The analysis is based on the memory address trace corresponding to* ***a particular execution order*** *of the operations constituting the computation.* Thus, it does not in any way account for the possibility of alternate valid execution orders for the computation that may exploit much better data locality. While reuse distance analysis provides a useful characterization of data locality for a given execution trace, it fails to provide any information on the potential for improvement in data locality that may be feasible through valid reordering of the operations in the execution trace.

In particular, given only the reuse distance profile for the address trace generated by execution of some code, it is not possible to determine whether the observed locality characteristics reveal fundamental inherent limitations of an algorithm, or are merely the consequence of a sub-optimal implementation choice.

In this paper, we develop a novel dynamic analysis approach to provide insights beyond that possible from standard reuse distance analysis. The analysis seeks to characterize the *inherent data locality potential* of the implemented algorithm, instead of the reuse distance profile of the address trace from a specific execution order of the constituent operations. We develop graph partitioning techniques that could be seen as a generalization of loop tiling, but considering arbitrary shapes for the tiles that enable atomic execution of tiles. Instead of simply performing reuse distance analysis on the execution trace of a given sequential program, we first explicitly construct a computational directed acyclic graph (CDAG) to capture the statement instances and their inter-dependences, next perform convex partitioning of the CDAG to generate a modified dependence-preserving execution order with better expected data reuse, and finally perform reuse distance analysis for the address

trace corresponding to the modified execution order. We apply the proposed approach on a number of benchmarks and demonstrate that it can be very effective.

This article makes the following contributions.

— It is the first work, to the best of our knowledge, to develop a dynamic analysis approach that seeks to characterize the inherent data locality characteristics of algorithms.
— It develops effective algorithms to perform convex partitioning of CDAGs to enhance data locality. While convex partitioning of DAGs has previously been used for estimating parallel speedup, to our knowledge this is the first effort to use it for characterizing data locality potential.
— It demonstrates the potential of the approach to identify opportunities for enhancement of data locality in existing implementations of computations. Thus, an analysis tool based on this approach to data locality characterization can be valuable to: (i) application developers, for comparing alternate algorithms and identifying parts of existing code that may have significant potential for data locality enhancement, and (ii) compiler writers, for assessing the effectiveness of a compiler's program optimization module in enhancing data locality of programs.
— It demonstrates, through case studies, the use of the new dynamic analysis approach in identifying opportunities for data locality optimization that are beyond the scope of the current state-of-the-art in optimizing compilers. For example, the insights from the analysis have resulted in the development of a 3D tiled version of the Floyd-Warshall all-pairs shortest paths algorithm, which was previously believed to be un-tileable without semantic information based transformations to the base algorithm.

The rest of the paper is organized as follows. Section 2 presents background on reuse distance analysis, and a high-level overview of the proposed approach for locality characterization. The algorithmic details of the approach to convex partitioning of CDAGs are provided in Section 3. Section 4 presents experimental results. Related work is discussed in Section 5, followed by concluding remarks in Sections 6 and 7.

2. BACKGROUND & OVERVIEW OF APPROACH

2.1. Reuse Distance Analysis

Reuse distance analysis is a widely used metric that models data locality [Mattson et al. 1970; Ding and Zhong 2003]. The reuse distance of a reference in a memory address trace is defined as the number of distinct memory references between two successive references to the same location.

Time	0	1	2	3	4	5	6	7	8	9
Data Ref.	d	a	c	b	c	c	e	b	a	d
Reuse Dist.	∞	∞	∞	∞	1	0	∞	2	3	4

Fig. 1: Example data reference trace

An example data reference trace of length $N = 10$ is shown in Fig. 1. It contains references to $M = 5$ distinct data addresses $\{a,b,c,d,e\}$. As shown in the figure, each reference to an address in the trace is associated with a reuse distance. The first time an address is referenced, its reuse distance is ∞. For all later references to an address, the reuse distance is the number of distinct intervening addresses referenced. In the figure, address c is referenced three times. Since b is referenced in between the first and second references to c, the latter has a reuse distance of 1. Since the second and third references to c are consecutive, without any other distinct intervening references to any other addresses, the last access to c has a reuse distance of 0.

A significant advantage of reuse distance analysis (RDA) is that a single analysis of the address trace of a code's execution can be used to estimate data locality characteristics as a function of the cache size. Given an execution trace, a reuse distance histogram for that sequence is obtained as follows. For each memory reference in the trace, say to location M, the reuse distance is the

number of distinct addresses referenced in the trace after the most recent preceding access to M (the reuse distance is considered to be infinity if there was no previous reference in the trace to M). The number of references in the trace with reuse distance of 0, 1, 2, ..., are counted to form the reuse distance histogram for the trace. A cumulative reuse distance histogram plots, as a function of k, the number of references in the trace that have reuse distance less than or equal to k. The cumulative reuse distance histogram directly provides the number of cache hits for a fully associative cache of capacity C with a LRU (Least Recently Used) replacement policy, since the data accessed by any reference with reuse distance less than or equal to C would still be present in such a cache.

Example. We use a simple example to illustrate both the benefits as well as a significant limitation of standard RDA. Fig. 2 shows code for a simple Seidel-like spatial sweep, with a default implementation as well as a fully equivalent tiled variant, where the computation is executed in blocks.

```
for(i = 1; i < N-1; i++)
  for(j = 1; j < N-1; j++)
    A[i][j] = A[i-1][j] + A[i][j-1];
```

(a) Untiled

```
/* B -> Tile size */
for(it = 1; it < N-1; it += B)
  for(jt = 1; jt < N-1; jt += B)
    for(i = it; i < min(it+B, N-1); i++)
      for(j = jt; j < min(jt+B, N-1); j++)
        A[i][j] = A[i-1][j] + A[i][j-1];
```

(b) Tiled

Fig. 2: Example: Single-sweep two-point Gauss-Seidel code

Fig. 3(a) displays the cumulative reuse distance histogram for both versions. As explained above, it can be interpreted as the number of data cache hits (y axis) as a function of the cache size (x axis). The same data is depicted in Fig. 3(b), showing the number of cache misses (by subtracting the number of hits from the total number of references).

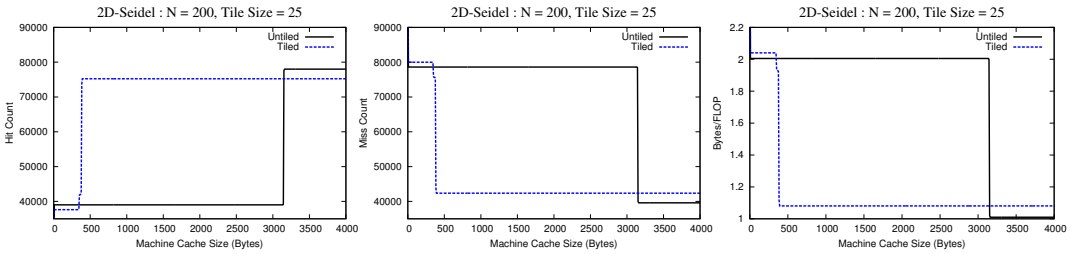


Fig. 3: Reuse distance profile: (a) cache hit rate, (b) cache miss rate, and (c) memory bandwidth demand for tiled/untiled versions of code in Fig. 2(a),(b)

From Fig. 3(a), we can conclude that with the untiled form of the code, a cache with capacity less than 400 words (3200 bytes, with 8 bytes per element) will be too small to effectively exploit reuse. The reuse distance profile for the tiled code is quite different, suggesting that effective exploitation of reuse is feasible with a very much smaller cache of capacity of 50 words (400 bytes). First we focus on the benefits of RDA illustrated by the example: i) For a given code, it provides insights into the impact of cache capacity on the expected effectiveness of data locality exploitation, and ii) Given two known alternative implementations for a computation, it enables a comparative assessment of the codes with respect to data locality.

Limitations of reuse distance analysis. The Seidel example also illustrates a fundamental shortcoming of RDA that we address through the work presented in this article: Given an execution trace for a code, RDA only provides a data locality characterization for one *particular execution order* of the constituent operations, and provides no insights on whether significant improvements may be possible via dependence preserving reordering of execution of the operations. The tiled and untiled variants in Fig. 2 represent equivalent computations, with the only difference being the relative order of execution of exactly the same set of primitive arithmetic operations on exactly the same sets of array operands. Although state-of-the-art static compiler transformation techniques (e.g., using polyhedral loop transformations) can transform the untiled code in Fig. 2(a) to a tiled form of Fig. 2(b), many codes exist (as illustrated through case studies later in this article), whose data locality characteristics can be improved, but are beyond the scope of the most advanced compilers today. The main question that RDA does not answer is whether or not a code with seemingly poor reuse distance profile could potentially be improved. In other words, is the poor reuse distance profile due to a sub-optimal execution order of the operations (e.g., untiled code version of a tileable algorithm) or is it more fundamental and relatively unchangeable through any transformations to change the execution order of the operations? This is the question our work seeks to assist in answering. By analyzing the execution trace of a given code, forming a dynamic data dependence graph, and reordering the operations by forming convex partitions, the potential for significantly improved reuse distance profile is evaluated. The change to the reuse distance profile after the dynamic analysis and reordering, rather than the shape of the initial reuse distance profile of a code, provides guidance on the potential for further improvement.

Fig. 3(c) presents the information in Fig. 3(b) in terms of memory bandwidth required per operation. It translates the cache miss count into the bandwidth demand on the memory system in bytes/second per floating-point operation. For this code, we have one floating point operation per two memory references. With a cache miss rate m, assuming double-precision (8 bytes per word), the demand on the main-memory bandwidth would be $16 * m$ bytes per Flop. If this ratio is significantly higher than the ratio of a system's main memory bandwidth (in Gbytes/sec) to its peak performance (in GFlops), the locality analysis indicates that achieving high performance will be critically dependent on effective data locality optimization. For example, on most current systems, the performance of this computation will be severely constrained by main memory bandwidth for problem sizes that are too large to fit in cache.

A point of note is that while estimated cache hit rates/counts by the use of RDA can deviate quite significantly from actually measured cache hit rates/counts on real systems (due to a number of aspects of real caches, such as non-unit line size, finite associativity, pre-fetching, etc.), the bytes/flop metric serves as a robust lower bound on the bandwidth requirement for real caches. This is because pre-fetching and non-unit line sizes only affect the latency and number of main memory accesses and not the minimum volume of data that must be moved from memory to cache. Finite cache associativity could cause an increase in the number of misses compared to a fully associative cache, but not a decrease. All the experimental results presented later in the article depict lower bounds on the bytes/flop bandwidth demanded by a code. Thus, despite the fact that RDA essentially models an idealized fully associative cache, the data represents valid lower bounds on the bandwidth demand for any real cache.

Benefits of the proposed dynamic analysis. Using results from two case studies presented later in the article, we illustrate the benefits of the dynamic analysis approach we develop. Fig. 4 shows the original reuse distance profiles as well as the profiles after dynamic analysis and convex partitioning, for two benchmarks: Householder transformation on the left, and Floyd-Warshall all-pairs shortest path on the right.

As seen in Fig. 4(a), with the Householder code, no appreciable change to the reuse distance profile results from the attempted reordering after dynamic analysis. In contrast, Fig. 4(b) shows a significantly improved reuse distance profile for the Floyd-Warshall code, after dynamic analysis and reordering of operations. This suggests potential for enhanced data locality via suitable code

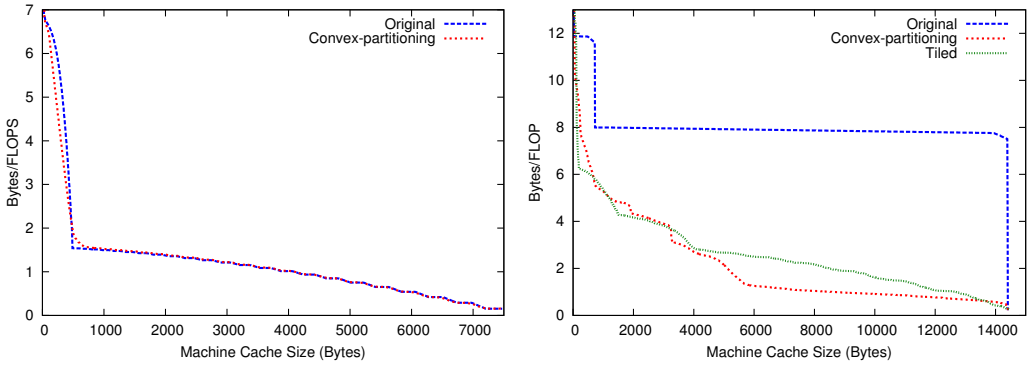


Fig. 4: Reuse distance analysis for (a) Householder (left) and (b) Floyd-Warshall (right)

transformations. As explained later in the experimental results section, indeed manual examination of the convex partitions provided insights into how the code could be transformed into an equivalent form that in turn could be tiled by an optimizing compiler. The reuse distance profile of that tiled version is shown as a third curve in Fig. 4(b), showing much better reuse than the original code. The actual performance of the modified code was also significantly higher than the original code. To the best of our knowledge, this is the first 3D tiled implementation of the Floyd Warshall algorithm (other blocked versions have been previously developed [Venkataraman et al. 2003; Park et al. 2004], but have required domain-specific reasoning for semantic changes to form equivalent algorithms that generate different intermediate values but the same final results as the standard algorithm).

2.2. Overview of Approach

The new dynamic analysis approach proposed in this paper attempts to characterize the inherent data locality properties of a given (sequential) computation, and to assess the potential for enhancing data locality via change of execution ordering. To achieve this goal, we proceed in two stages. First, a new ordering of the program's operations is computed, by using graph algorithms (that is, convex partitioning techniques) operating on the expanded computation graph. Then, standard reuse distance analysis is performed on the reordered set of operations. We note that our analysis does not directly provide an optimized program. Implementing the (possibly very complex) schedule found through our graph analysis is impractical. Instead, our analysis highlights gaps between the reuse distance profile of a current implementation and existing data locality potential: the task of devising a better implementation is left to the user or compiler writer. In Sec. 4, we illustrate the benefits of the approach on several case study benchmarks.

To implement our new dynamic analysis, we first analyze the data accesses and dependences between the primitive operations in a sequential execution trace of the program to extract a more abstract model of the computation: a computational directed acyclic graph (CDAG), where operations are represented as vertices and the flow of values between operations as edges. This is defined as follows.

Definition 2.1 (*CDAG [Bilardi and Peserico 2001]*). A computation directed acyclic graph (CDAG) is a 4-tuple $C = (I,V,E,O)$ of finite sets such that: (1) $I \cap V = \emptyset$; (2) $E \subseteq (I \cup V) \times V$ is the set of arcs; (3) $G = (I \cup V, E)$ is a directed acyclic graph with no isolated vertices; (4) I is called the input set; (5) V is called the operation set and all its vertices have one or two incoming arcs; (6) $O \subseteq (I \cup V)$ is called the output set.

Fig. 5 shows the CDAG corresponding to the code in Fig. 2 for N=6 — both versions have identical CDAGs since they perform exactly the same set of floating-point computations, with the

same inter-instance data dependences, even though the total order of execution of the statement instances is different. The loop body performs only one addition and is executed a total of 16 times, so the CDAG has 16 computation nodes (white circle).

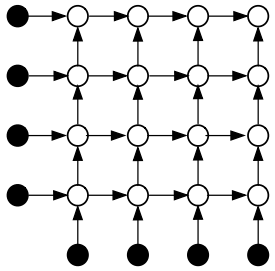


Fig. 5: CDAG for Gauss-Seidel code in Fig. 2. Input vertices are shown in black, all other vertices represent operations performed.

Although a CDAG is derived from analysis of dependences between instances of statements executed by a sequential program, it abstracts away that sequential schedule of operations and only imposes an essential partial order captured by the data dependences between the operation instances. Control dependences in the computation need not be represented since the goal is to capture the inherent data locality characteristics based on the set of operations that actually transpired during an execution of the program.

They key idea behind the work presented in this article is to perform analysis on the CDAG of a computation, attempting to find a different order of execution of the operations that can improve the reuse-distance profile compared to that of the given program's sequential execution trace. If this analysis reveals a significantly improved reuse distance profile, it suggests that suitable source code transformations have the potential to enhance data locality. On the other hand, if the analysis is unable to improve the reuse-distance profile of the code, it is likely that it is already as well optimized for data locality as possible.

The dynamic analysis involves the following steps:

(1) Generate a sequential execution trace of a program.
(2) Form a CDAG from the execution trace.
(3) Perform a multi-level convex partitioning of the CDAG, which is then used to change the schedule of operations of the CDAG from the original order in the given input code. A convex partitioning of a CDAG is analogous to tiling the iteration space of a regular nested loop computation. Multi-level convex partitioning is analogous to multi-level cache-oblivious blocking.
(4) Perform standard reuse-distance analysis of the reordered trace after multi-level convex partitioning.

Finally, Fig. 6 shows the convex partitioning of the CDAG corresponding to the code in Fig. 2.

After such a partitioning, the execution order of the vertices is reordered so that the convex partitions are executed in some valid order (corresponding to a topological sort of a coarse-grained inter-partition dependence graph), with the vertices within a partition being executed in the same relative order as the original sequential execution. Details are presented in the next section.

3. CONVEX PARTITIONING OF CDAG

In this section, we provide details on our algorithm for convex partitioning of CDAGs, which is at the heart of our proposed dynamic analysis. In the case of loops, numerous efforts have attempted to optimize data locality by applying loop transformations, in particular involving loop tiling and

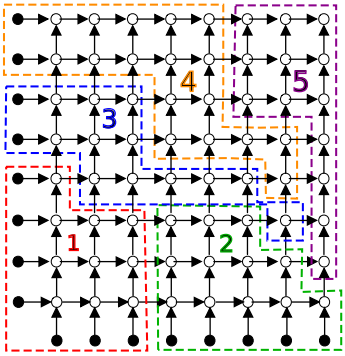


Fig. 6: Convex-partition of the CDAG for the code in Fig. 2 for problem size $N = 10$.

loop fusion [Irigoin and Triolet 1988; Wolf and Lam 1991; Kennedy and McKinley 1993; Bondhugula et al. 2008]. Tiling for locality attempts to group points in an iteration space of a loop into smaller blocks (tiles) allowing reuse (thereby reducing reuse distance) in multiple directions when the block fits in a faster memory (registers, L1, or L2 cache). Forming a valid tiling for a loop requires that each tile can be executed atomically, i.e., each tile can start after performing required synchronizations for the data it needs, then execute all the iterations in the tile without requiring intervening synchronization. This means that there are no cyclic data dependencies between any two tiles. *Our goal in this work is to extend this notion of "tiling" to arbitrary CDAGs that represent a computation: we form valid partitioning of CDAGs into components such that the components can be scheduled and executed, with all vertices in a component being executed "atomically," i.e., without being interleaved with vertices in any other components.* For this, we rely on the notion of *convex partitioning* of CDAGs, which is the generalization of loop tiling to graphs.

3.1. Definitions

We first define what is a convex component, that is a tile in a graph.

Definition 3.1 (*Convex component*). Given a CDAG G, a convex component V_i in G is defined as a subset of the vertices of G such that, for any pair of vertices u and v in V_i, if there are paths between u and v in G, then every vertex on every path between u and v also belongs to V_i.

A convex partition of a graph G is obtained by assigning each vertex of G to a single convex component. Since there are no cycles among convex components, the graph in which nodes are convex components and edges define dependences among them, is acyclic. Therefore, we can execute the convex components using any topologically sorted order. Executing all the convex components results in executing the full computation.

A *convex partition* of a graph $G = (V,E)$ is a collection of convex components $\{V_1,\ldots,V_k\}$ of G such that $\bigcup_{i=1}^{k} V_i^k = V$ and for any i,j s.t. $1 \leq i,j \leq k$ and $i \neq j$, $V_i \cap V_j = \emptyset$. We remark that tiling of iterations spaces of loops results in convex partitions.

The *component graph* $\mathcal{C} = (\mathcal{V}_\mathcal{C}, \mathcal{E}_\mathcal{C})$ is defined as a graph whose vertices $\mathcal{V}_\mathcal{C}$ represent the convex components, i.e., $\mathcal{V}_\mathcal{C} = \{V_1,\cdots,V_k\}$. Given two distinct components V_i and V_j, there is an edge in $\mathcal{C}$ from V_i to V_j if and only if there is an edge (a,b) in the CDAG, where $a \in V_i$ and $b \in V_j$.

For a given schedule of execution of the vertices of convex component V_i, we define *maxlive* to be the maximum number of simultaneously live node for this schedule. A node can be in one of the following states throughout its life: *(initial state)* at the beginning no node is live; *(birth)* any node is considered live right after it is fired (executed); *(resurrection)* if not part of the convex component, it is also considered as live when used by another node of the component (predecessor of a fired node belonging to the component); *(live)* a born or resurrected node stays alive until it dies, which

happens if all its successor nodes have executed (are part of the partition); *(death)* a node dies right after its last successor fires.

Our goal is to form convex components along with a scheduling such that the *maxlive* of each component does not exceed the local memory capacity. We consider the nodes we add to the component (just fired and alive), and their predecessors (resurrected) in computing the *maxlive*.

3.2. Forming Convex Partitions

We show in Algorithm 1 our technique to build convex partitions from an arbitrary CDAG. It implements a convex-component growing heuristic that successively adds ready vertices into the component until a capacity constraint is exceeded. The key requirement in adding a new vertex to a convex component is that if any path to that vertex exists from a vertex in the component, then all vertices in that path must also be included. We avoid an expensive search for such paths by constraining the added vertices to be those that already have all their predecessors in the current (or previously formed) convex component.

The partitioning heuristic generates a valid schedule as it proceeds. At the beginning, all input vertices to the CDAG are placed in a ready list R. A vertex is said to be *ready* if all its predecessors (if any) have already executed, i.e., have been assigned to some convex component. A new convex component cc is started by adding a ready vertex to it (the function `selectReadyNode`(R) simply picks up one element of R) and it grows by successively adding more ready nodes to it (`selectBestNode`(R, cc, CF) selects one of the ready nodes, as shown in Algorithm 4 – the criterion is described later). Suppose a vertex n is just added to a component cc. As a result, zero or more of the successors of n in G may become ready: a successor s of n becomes ready if the last predecessor needed to execute s is n.

ALGORITHM 1: GenerateConvexComponents(G, C, CF)

```
Input : G : CDAG; C : Cache Size;
        CF: Cost function to decide next best node
InOut: P : Partition containing convex components
begin
    P ⟵ ∅
    R ⟵ getTheInitialReadyNodes(G)
    while R ≠ ∅ do
        n ⟵ selectReadyNode(R)
        cc ⟵ ∅
        while R ≠ ∅ ∧ updateLiveSet(cc, n, C) do
            cc ⟵ cc ∪ {n}
            R ⟵ R − {n}
            UpdateListOfReadyNodes(R, n)
            n ⟵ selectBestNode(R, cc, CF, n)
        P ⟵ P ∪ {cc}
```

The addition of newly readied vertices to the ready list is done by the function `updateListOfReadyNodes`(R, n), as shown in Algorithm 2. In this function, the test that checks if s has unprocessed predecessors is implemented using a counter that is updated whenever a node is processed.

Before adding a node to cc, the set $cc.liveset$, the liveout set of cc, is updated through the call to `updateLiveSet`(p, n, C), as shown in Algorithm 3. `updateLiveSet` exactly implements our definition of liveness previously described: *(birth)* if n has some successors it is added to the liveset of cc; *(resurrect)* its predecessor nodes that still have unprocessed successors are added to the liveset (if not already in it); *(die)* predecessor nodes for which n is the last unprocessed successor are removed from the liveset.

ALGORITHM 2: UpdateListOfReadyNodes(R, n)

Input : n: Latest processed node
InOut: R: List of ready nodes
begin
  for $s \in$ `successors(`n`)` **do**
    if *s has no more unprocessed predecessors* **then**
      $R \longleftarrow R \cup \{s\}$

3.3. CDAG Traversal: Breadth-first Versus Depth-first

The heuristic to select the next processed node within the ready list uses two affinity notions: a node is a ready-successor of cc (thus element of the *cc.readySuccessors* list) if it is a ready successor of some nodes of cc; a node is a ready-neighbor of cc (thus element of *cc.readyNeighbors* list) if it has a successor node that is also a successor of some node in cc. We note that those two lists can overlap. The growing strategy picks up ready nodes, using a first-in first-out policy, from one of those two lists. In practice, we observe that favoring nodes of the ready-successor list would favor growing depth-first in the CDAG, while favoring nodes that belongs to the ready-neighbor list would favor a breadth-first traversal.

The heuristic uses a combination of growing alternately in these two different directions till the *Maxlive* of the component exceeds the capacity of the cache. The priority is controlled by a number that represents the ratio of selected ready-neighbors over selected ready-successors. If the ratio is larger than 1, we refer to it as *breadth-priority*; if lower than 1, we refer to it as *depth-priority*, otherwise it is referred to as *equal-priority*.

ALGORITHM 3: updateLiveSet(p, n, C)

Input : n : New node added in the partition p
  C : Cache size
InOut : $p.liveset$: Live set of p
Output: true if $|p.liveset| \leq C$, false otherwise
begin
  $lset \longleftarrow p.liveset$
  if *n has unprocessed successors* **then**
    $p.liveset \longleftarrow p.liveset \cup \{n\}$
  for $n' \in$ `predecessors(`n`)` **do**
    if *n' has unprocessed successors* **then**
      $p.liveset \longleftarrow p.liveset \cup \{n'\}$
    else if $n' \in p.liveset$ **then**
      $p.liveset \longleftarrow p.liveset - \{n'\}$
  if $|lset| > C$ **then**
    return false
  $p.liveset \longleftarrow lset$
  return true

3.4. Multi-level Cache-oblivious Partitioning

Here we address the problem of finding a schedule that is cache-size oblivious, and in particular suitable for multi-level memory hierarchy. In order to address this problem, we construct a hierarchical partitioning using the multi-level component growing heuristic shown in Algorithm 5. This

ALGORITHM 4: selectBestNode(*R, cc, priority, n*)

Input : *R*: List of ready nodes
cc: current convex component
priority: Give priority to neighbor or successor
n: Latest node added in the partition
InOut : *cc.readyNeighbors* : Ready neighbors of current growing partition nodes
cc.readySuccessors : Ready successors of current growing partition nodes
Output: *next* : Next node to add in the partition

```
begin
    for a ∈ neighbors(n) ∩ R − cc.readyNeighbors do
        cc.readyNeighbors.enqueue(a)
    for a ∈ successors(n) ∩ R − cc.readySuccessors do
        cc.readySuccessors.enqueue(a)
    cc.readyNeighbors ⟵ cc.readyNeighbors − n
    cc.readySuccessors ⟵ cc.readySuccessors − n
    if cc.takenNeighbors < cc.takenSuccessors × priority
            ∧ cc.readyNeighbors ≠ ∅ then
        next ⟵ dequeue(cc.readyNeighbors)
        cc.takenNeighbors ⟵ cc.takenNeighbors + 1
    else if cc.readySuccessors ≠ ∅ then
        next ⟵ dequeue(cc.readySuccessors)
        cc.takenSuccessors ⟵ cc.takenSuccessors + 1
    else
        next ⟵ selectReadyNode(R)
    return next
```

algorithm combines individual components formed for a cache of size C using the heuristic in Algorithm 1 to form components for a cache of size factor * C. In this approach, each component of the partition built at level l of the heuristic is seen as a single node at level $l+1$. We call these nodes "macro-nodes" as they typically represent sets of nodes in the original CDAG.

This approach could be compared with multi-level tiling for multi-level cache hierarchy, a classical scheme to optimize data locality for multi-level caches. For the first level of this heuristic, a macro-node corresponds to a node in the original CDAG. The heuristic then proceeds with the next level, seeing each component of the partition at the previous level as a macro-node at the current level. The heuristic stops when only one component is generated at the current level, that is, all macro-nodes were successfully added to a single convex component without exceeding the input/output set size constraints. The number of levels in the multi-level partitioning varies with each CDAG, and is not controlled by the user. When a component cc_0 formed at a lower level is added to the current component cc_1 being formed at a higher level, the *liveset* of cc_1 has to be updated, just as if all the nodes composing cc_0 have been added to cc_1. This leads to the modified version of `updateLiveSet`(*p,n,C*) reported in Algorithm 6, where the function `FirstLevelBaseNodes`(*np*) returns the actual CDAG nodes (that we call first level base nodes) that the macro-node *np* is actually build upon. At the first level `FirstLevelBaseNodes`(*np*) may be understood as returning just *np*.

Complexity Analysis. The overall complexity of the single-level version is thus linear with the size of the trace. The multi-level version is run $\log_{factor}\left(\frac{|M|}{|C|}\right)$ times `GenerateConvexComponents`, thus leading to an overall time complexity of $O(|T|\log(|M|))$. A step-by-step analysis of the complexity of our analysis can be found in [Fauzia et al. 2013].

ALGORITHM 5: MultiLevelPartitioning(*G, C, Priority, factor*)

Input : G : CDAG
C : initial cache Size
Priority : priority to Neighbor or Successor
factor : multiplication factor of Cache size for each level
InOut : $G.M$: memory footprint of the CDAG
Output: P : Final single partition
begin
  $P \longleftarrow$ `GenerateConvexComponents`(*G, C, Priority*)
  while $C < G.M$ **do**
    $G' \longleftarrow$ `formMacroNodeWithEachPartition`(*P, G*)
    $C \longleftarrow factor * C$
    $P' \longleftarrow$ `GenerateConvexComponents`(G', *C, Priority*)
    $P \longleftarrow P'$
  return P

ALGORITHM 6: updateLiveSet(*p, n, C*)

Input : n : New macro-node added in the partition p
InOut : $p.liveset$: Live set of p
Output: true if $|p.liveset| \leq C$, false otherwise
begin
  $b \longleftarrow$ true
  $plset \longleftarrow p.liveset$
  for $nb \in$ `FirstLevelBaseNodes`(n) **do**
    $b \longleftarrow b \wedge$ `updateLiveSet`(*p, nb, C*)
  if $b = false$ **then**
    $p.liveset \longleftarrow plset$
    return false
  return true

4. EXPERIMENTAL RESULTS

The experimental results are organized in two major parts. In Sec. 4.2 we evaluate the impact of the various parameters of the convex partitioning heuristics, using two well understood benchmarks: matrix multiplication and a 2D Jacobi stencil computation. With these benchmarks, it is well known how the data locality characteristics of the computations can be improved via loop tiling. The goal therefore is to assess how the reuse distance profiles after dynamic analysis and operation reordering compares with the unoptimized untiled original code as well as the optimized tiled version of code.

In Sec. 4.3 we detail several case studies where we use dynamic analysis to characterize the locality potential of several benchmarks for which the state-of-the-art optimizing compilers are unable to automatically optimize data locality. We demonstrate the benefits of dynamic analysis in providing insights into the inherent data locality properties of these computations and the potential for data locality enhancement. Finally we discuss in Sec. 4.4 the sensitivity of our techniques to varying datasets.

4.1. Experimental Setup

The dynamic analysis we have implemented involves three steps. For the CDAG Generation, we use automated LLVM-based instrumentation to generate the sequential execution trace of a program, which is then processed to generate the CDAG. The trace generator was previously developed for performing dynamic analysis to assess vectorization potential in applications [Holewinski et al. 2012]. For the convex partitioning of the CDAG, we have implemented the algorithms explained in

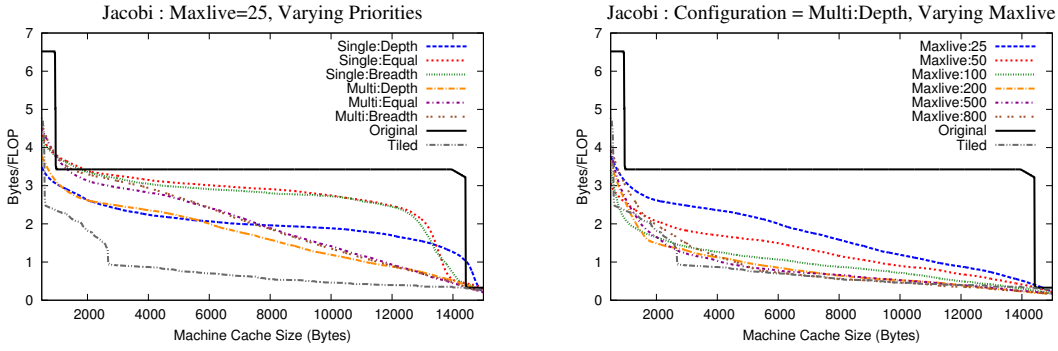
detail in the previous section. Finally for the reuse distance analysis of the reordered address trace after convex partitioning, it is done using a parallel reuse distance analyzer PARDA [Niu et al. 2012] that was previously developed.

The total time taken to perform the dynamic analysis is dependent on the input program trace size. In our experiments, computing the trace and performing the full dynamic analysis can range between seconds for benchmarks like Givens, Householder, odd-even sort or Floyd-Warshall to about one hour for SPEC benchmarks such as 420.LBM. For instance, for Givens rotation (QR decomposition) the trace is built in 4 seconds, the analysis takes another 14 seconds, and computing the reuse distance analysis on the partitioned graph takes well below a second. We note that while CDAGs are often program-dependent, the shape of the CDAG and the associated dynamic analysis reasoning performed can usually be performed on a smaller problem size: the conclusion about the data locality potential is likely to hold similarly on the same program running on larger datasets. A study of the impact of the sensitivity of our analysis to different datasets is provided in later Sec. 4.4. All performance experiments were done on an Intel Core i7 2700K, using a single core.

4.2. Impact of Heuristic Parameters

The convex partitioning heuristic two parameters. First the *Search Startegy*: this includes (a) prioritization in selecting a new vertex to include in a convex partition: depth-priority, breadth-priority, or alternation between depth and breadth priority (equal priority); and (b) single level partitioning versus multi-level partitioning. The second is *Maxlive*: the parameter that sets a limit on the maximum number of live vertices allowed while forming a partition.

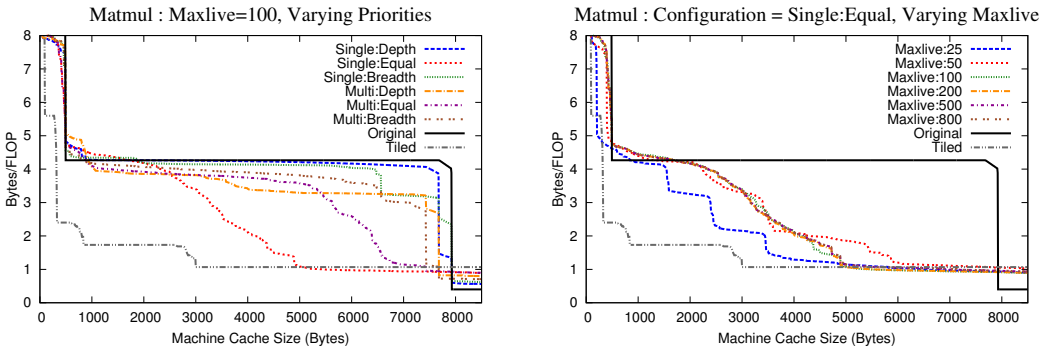
4.2.1. Jacobi 2D. Fig. 7 presents the results of applying the dynamic analysis on a Jacobi stencil on a regular 2-dimensional grid of size 32, and 30 time iterations. Fig. 7(a) shows reuse distance profiles for a fixed value of *Maxlive* and different configurations for single versus multi-level partitioning, and different priorities for next node selection. With single-level partitioning, depth-priority is seen to provide the best results. Using multi-level partitioning further improves the reuse distance profile. In order to judge the effectiveness of the convex partitioning in improving the reuse distance profile, we show both the reuse distance profiles for the original code and an optimally tiled version of the Jacobi code. It can be seen that there is significant improvement over the original code, but still quite some distance from the profile for the tiled code. Fig. 7(b) shows the effect of varying *Maxlive* from 25 to 800, with multi-level depth-priority partitioning. Here it can be seen that at large values of *Maxlive*, the profile is very close to that of the optimized tiled code. Thus, with a large value of *Maxlive* and use of multi-level depth-priority partitioning, the convex partitioning heuristic is very effective for the Jacobi-2D benchmark.



(a) (b)

Fig. 7: Results with different heuristics for Jacobi-2D

4.2.2. Matrix Multiplication. Fig. 8 shows experimental results for matrix multiplication, for matrices of size 30 by 30. In Fig. 8(a), the selection priority is varied, for single and multi-level partitioning. In contrast to the Jacobi benchmark, for Matmult, equal priority works better than breadth or depth priority. Further, single level partitioning provides better results than multi-level partitioning. In Fig. 8(b), we see performance variation as a function of *Maxlive* for single-level equal-priority partitioning. Again the trends are quite different from those of Jacobi-2D: the best results are obtained with the lowest value of 25 for *Maxlive*.



(a) (b)

Fig. 8: Results with different heuristics for matrix multiplication

These results suggest that no single setting of parameters for the convex partitioning heuristic is likely to be consistently effective across benchmarks. We conjecture that there may be a relationship between graph properties of the CDAGs (e.g., low fan-out vs. high fan-out) and the best parameters for the partitioning heuristic.

For Matmul, the tiled code has a better reuse distance profile than the best reported heuristic in Fig. 8. This may happen, in particular when the tiled implementation achieves the provably optimal I/O lower bound, which is the case for Matmult here. Our heuristics for building convex partitions use several simplifications to improve scalability, in particular in how the candidates to be inserted in a partition are chosen, and in how the obtained partitions are scheduled. In addition, we do not explore the Cartesian product of all possible parameters values (priority and maxlive values) but instead limit to a reasonable subset, again for scalability purposes. These factors all contribute to our analysis possibly under-estimating the data locality potential of the application. We disuss in Sec. 6 the tightness of our analysis and what complementary techniques could be used to assess the quality of our heuristics.

4.3. Case Studies

We next present experimental results from applying dynamic analysis to several benchmarks: the Floyd-Warshall algorithm to find all-pairs shortest path in a graph represented with an adjacency matrix, two QR decomposition methods: the Givens rotation and the Householder transformation, three SPEC benchmarks, a LU decomposition code from the LAPACK package, and an implementation of odd-even sorting using linked list. None of these benchmarks could be fully tiled for enhanced data locality by state-of-the art research compilers (e.g., Pluto [pluto]) or production compilers (e.g., Gnu GCC, Intel ICC). For each benchmark, we study the reuse distance profile of the original code and the code after convex partitioning. Where significant potential for data locality enhancement was revealed by the dynamic analysis, we performed a careful analysis of the code to make changes. For two of the four analyzed benchmarks (namely, Floyd-Warshall and Givens rotation), the modified code was successfully maximally tiled, providing a significant performance improvement over the original code.

4.3.1. Floyd-Warshall.

Original program. We show in Fig. 9 the original input code that we used to implement the Floyd-Warshall algorithm. We refer to this code as "out-of-place" Floyd-Warshall because it uses a temporary array to implement the all-pairs shortest path computation.

```
for (k = 0; k < N; k++) {
  for (i = 0; i < N; i++)
    for (j = 0; j < N; j++)
      temp[i][j] = MIN(A[i][j], (A[i][k] + A[k][j]));
  k++;
  for (i = 0; i < N; i++)
    for (j = 0; j < N; j++)
      A[i][j] = MIN(temp[i][j], (temp[i][k] + temp[k][j]));
}
```

Fig. 9: Floyd-Warshall all-pairs shortest path

Analysis. Fig. 10 shows the reuse distance profile of the original code and the convex-partitioning for the Floyd-Warshall algorithm, for a matrix of size 30 by 30. As we can see from Fig. 10, the convex-partitioning heuristics show that there is potential for improvement of data locality through transformations.

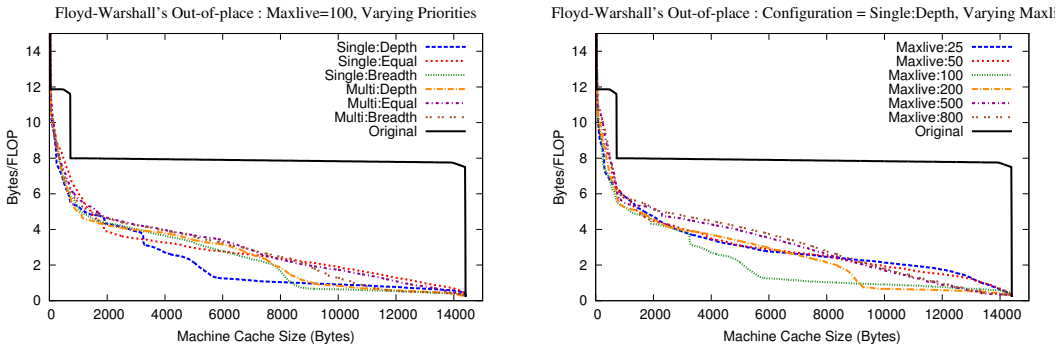


Fig. 10: Results with different heuristics for Floyd-Warshall's algorithm

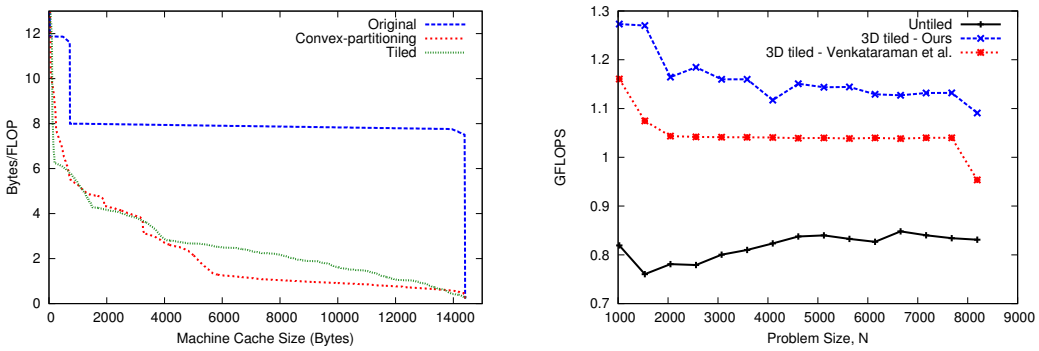
Indeed, the Floyd-Warshall algorithm is immediately tilable, along the two loops `i` and `j`. Such tiling can for instance be achieved automatically with polyhedral model based compilers such as Pluto [Bondhugula et al. 2008]. Since the three loops are not fully permutable, it has been believed that the Floyd-Warshall code cannot be 3D-tiled without transformations using semantic properties of the algorithm to create a modified algorithm (i.e., with a different CDAG) that provably produces the same final result [Venkataraman et al. 2003; Park et al. 2004]. However, a careful inspection of the convex partitions revealed that *valid 3D tiles can be formed among the operations of the standard Floyd-Warshall algorithm*. This non-intuitive result comes from the non-rectangular shape of the tiles needed, with varying tile size along the `k` dimension as a function of the value of `k`. This motivated us to look for possible transformations that could enable 3D tiling of the code without any semantic transformations.

Modified implementation. Fig. 11 shows the tiled version of the code that is exactly equivalent to the code in Listing 9 (i.e., has an identical CDAG). Tiling was enabled through manual index-set splitting of the iteration space into four regions as indicated in Listing 11.

```
/*Region 4*/
for (k = 0; k < N; k+=B1)
  for (i = k, iend = N; i < iend; i+=B2)
    for (j = k, jend = N; j < jend; j+=B3)
      for(kt = k, ktend = MIN(k+B1,N); kt < ktend; ++kt) {
        for(it = MAX(i,kt), itend = MIN(i+B2,N); it < itend; ++it)
          for(jt = MAX(j,kt), jtend = MIN(j+B3,N); jt < jtend; ++jt)
            temp[it][jt] = MIN(A[it][jt], (A[it][kt] + A[kt][jt]));
        ++kt;
        for(it = MAX(i,kt), itend = MIN(i+B2,N); it < itend; ++it)
          for(jt = MAX(j,kt), jtend = MIN(j+B3,N); jt < jtend; ++jt)
            A[it][jt] = MIN(temp[it][jt], (temp[it][kt] + temp[kt][jt]));
      }

/*Region 3*/
for (k = 0; k < N; k+=B1)
  for (i = k, iend = N; i < iend; i+=B2)
    for(j = 0, jend = k+B1; j<jend; j+=B3)
      for(kt = k, ktend = MIN(k+B1,N); kt < ktend; ++kt) {
        for(it = MAX(i,kt), itend = MIN(i+B2,N); it < itend; ++it)
          for(jt = j, jtend = MIN(j+B3,kt); jt < jtend; ++jt)
            temp[it][jt] = MIN(A[it][jt], (A[it][kt] + A[kt][jt]));
        ++kt;
        for(it = MAX(i,kt), itend = MIN(i+B2,N); it < itend; ++it)
          for(jt = j, jtend = MIN(j+B3,kt); jt < jtend; ++jt)
            A[it][jt] = MIN(temp[it][jt], (temp[it][kt] + temp[kt][jt]));
      }

/*Region 2*/
for(k = 0; k < N; k+=B1)
  for(i = 0, iend = k+B1; i<iend; i+=B2)
    for(j = k, jend = N; j<jend; j+=B3)
      for(kt = k, ktend = MIN(k+B1,N); kt < ktend; ++kt) {
        for(it = i, itend = MIN(i+B2,kt); it < itend; ++it)
          for(jt = MAX(j,kt), jtend = MIN(j+B3,N); jt < jtend; ++jt)
            temp[it][jt] = MIN(A[it][jt], (A[it][kt] + A[kt][jt]));
        ++kt;
        for(it = i, itend = MIN(i+B2,kt); it < itend; ++it)
          for(jt = MAX(j,kt), jtend = MIN(j+B3,N); jt < jtend; ++jt)
            A[it][jt] = temp[it][jt] + (temp[it][kt] + temp[kt][jt]);
      }

/*Region 1*/
for(k = 0; k < N; k+=B1)
  for(i = 0, iend = k+B1; i<iend; i+=B2)
    for(j = 0, jend = k+B1; j<jend; j+=B3)
      for(kt = k, ktend = MIN(k+B1,N); kt < ktend; ++kt)  {
        for(it = i, itend = MIN(i+B2,kt); it < itend; ++it)
          for(jt = j, jtend = MIN(j+B3,kt); jt < jtend; ++jt)
            temp[it][jt] = MIN(A[it][jt], (A[it][kt] + A[kt][jt]));
        ++kt;
        for(it = i, itend = MIN(i+B2,kt); it < itend; ++it)
          for(jt = j, jtend = MIN(j+B3,kt); jt < jtend; ++jt)
            A[it][jt] = MIN(temp[it][jt], (temp[it][kt] + temp[kt][jt]));
      }
```

Fig. 11: Tiled Floyd-Warshall implementation

Performance comparison. Fig. 12 compares the performance of the tiled version against the original code. From figure 12a, we can observe that the tiled code is able to achieve better data locality, that is close to the potential uncovered by the convex partitioning heuristics. Figure 12b shows the



(a) (b)

Fig. 12: Floyd-Warshall: Performance improvements due to tiling

improvement in actual performance of our tiled code (3D tiled - Ours), due to reduced cache misses. A performance improvement of about 1.6× (sequential execution) is achieved, across a range of problem sizes. Further, to the best of our knowledge, this is the first development of a tiled version of the standard Floyd-Warshall code that preserves the original code's CDAG. We also show the performance achieved by the semantically modified 3D-tiled implementation from [Venkataraman et al. 2003] in Fig. 12b, which has a slightly lower performance than our implementation.

4.3.2. Givens Rotation.

Original program. We show in Fig. 13 the original input code for the Givens rotation method used for QR decomposition.

```
for (j = 0; j < N; j++) {
  for (i = M-2; i >= j; i--) {
    double c =  A[i][j] / sqrt(A[i][j]*A[i][j] + A[i+1][j]*A[i+1][j]);
    double s = -A[i+1][j] / sqrt(A[i][j]*A[i][j] + A[i+1][j]*A[i+1][j]);
    for (k = j; k < N; k++) {
      double t1 = c * A[i][k] - s * A[i+1][k];
      double t2 = s * A[i][k] + c * A[i+1][k];
      A[i][k]   = t1;
      A[i+1][k] = t2;
    }
  }
}
```

Fig. 13: Givens Rotation

Analysis. Fig. 14 shows the reuse distance profile of the original code and after convex-partitioning for the Givens rotation algorithm, for an input matrix of size 30 by 30.

The convex partitioning analysis shows good potential for data locality improvement. Similarly to Floyd-Warshall, this code can be automatically tiled by a polyhedral-based compiler [Bondhugula et al. 2008], after implementing simple loop normalization techniques. However, this is not sufficient to tile all dimensions. Subsequent transformations are needed, as shown below.

Modified implementation. Based on the indicated potential for data locality enhancement, the code in Listing 13 was carefully analyzed and then manually modified to increase the applicability of automated tiling techniques. Fig. 15 shows this modified version. The modified code was obtained by first applying loop normalization [Kennedy and Allen 2002] which consists in making all loops

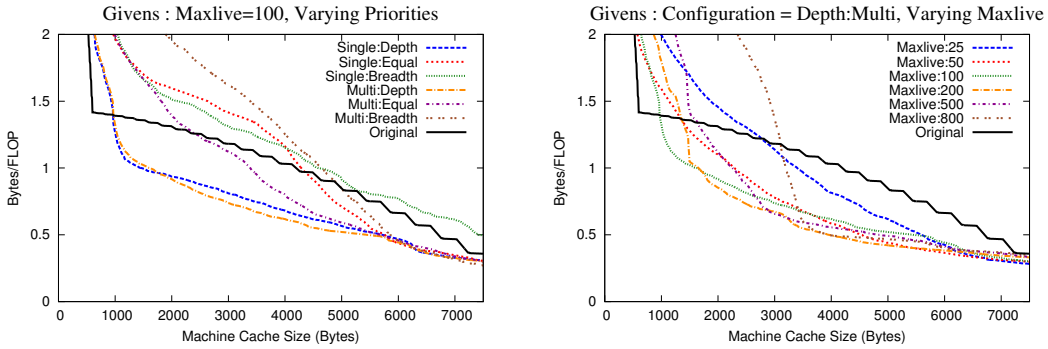


Fig. 14: Results with different heuristics for Givens Rotation

iterate from 0 to some greater value, and modifying accordingly the expressions involving the loop iterators in the code. Then, we applied scalar expansion on `c` and `s` [Kennedy and Allen 2002] to remove dependences induced by those scalars which were making loop permutation illegal. As a result, the modified code is an affine code with fewer dependences, enabling it to be automatically tiled by the Pluto compiler [pluto]. We applied Pluto on the modified code, using default tile sizes. The final tiled code obtained is shown in Fig. 16.

```
for (j = 0; j < N; j++) {
  for (i = 0; i <= M-2 - j; i++) {
    c[i][j] =  A[(M-2) - (i)][j]    / sqrt(A[(M-2) - (i)][j]*A[(M-2) - (i)][j]
                          + A[(M-2) - (i)+1][j]*A[(M-2) - (i)+1][j]);
    s[i][j] = -A[(M-2) - (i)+1][j] / sqrt(A[(M-2) - (i)][j]*A[(M-2) - (i)][j]
                          + A[(M-2) - (i)+1][j]*A[(M-2) - (i)+1][j]);
    for (k = j; k < N; k++) {
      A[(M-2) - (i)][k]   = c[i][j] * A[(M-2) - (i)][k] - s[i][j] * A[(M-2) - (i)+1][k];
      A[(M-2) - (i)+1][k] = s[i][j] * A[(M-2) - (i)][k] + c[i][j] * A[(M-2) - (i)+1][k];
    }
  }
}
```

Fig. 15: Modified Givens Rotation

Performance comparison. Fig. 17a shows the improvements in the reuse distance profile using the convex partitioning heuristics and for the improved reuse distance profile obtained from the tiled code. A better profile is obtained for the tiled version than for convex partitioning. Similarly as for Matmult, this is explained by the fact that our convex partitioning heuristic makes simplification for scalability and therefore is not guaranteed to provide the best achievable reuse profile.

The actual improvement in performance of the transformed code is shown in figure 17b. A performance improvement (sequential execution) of almost 2x is achieved, for matrices of size 4000.

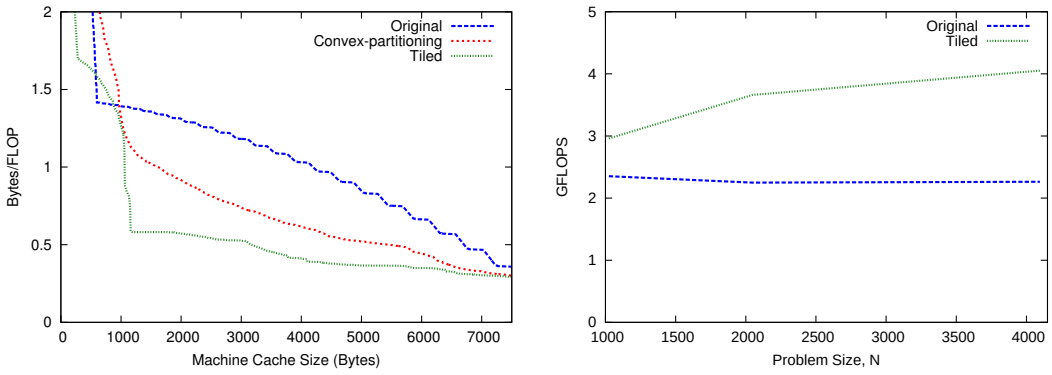
4.3.3. Householder Transformation.

Original program. We show in Fig. 18 the original input code for the Householder transform, another approach for QR decomposition.

Householder and Givens are two different approaches to compute a QR decomposition. Comparing these two algorithms in terms of data locality potential is of interest: if one has better locality potential than the other, then it would be better suited for deployment on machines where the data movement cost is the bottleneck. It complements complexity analysis, which only characterizes the

```
if (((M >= 2) && (N >= 1))) {
 for (c0 = 0; c0 <= min(floord((M + -2), 256),floord((N + -1),256));c0++){
  for (c1 = c0; c1 <= floord((M + -2), 256); c1++) {
   for (c2 = c0; c2 <= floord((N + -1), 256); c2++) {
    if ((c0 == c2)) {
     for (c3 = (256*c0); c3 <= min(min((M + -2),(N + -1)),((256*c0) + 255));c3++){
      for (c4 = max((256*c1),c3); c4 <= min((M + -2),((256*c1) + 255));c4++){
       c[((-1 * c3) + c4)][c3] = A[(M-2)-(((-1 * c3) + c4))][c3]
                                 /sqrt(A[(M-2)-(((-1 * c3) + c4))][c3]
                                  * A[(M-2)-(((-1 * c3) + c4))][c3]
                                  + A[(M-2)-(((-1 * c3) + c4))+1][c3]
                                  * A[(M-2)-(((-1 * c3) + c4))+1][c3] );
       s[((-1 * c3) + c4)][c3] = -A[(M-2)-(((-1 * c3) + c4))+1][c3]
                                 /sqrt(A[(M-2)-(((-1 * c3) + c4))][c3]
                                  * A[(M-2)-(((-1 * c3) + c4))][c3]
                                  + A[(M-2)-(((-1 * c3) + c4))+1][c3]
                                  * A[(M-2)-(((-1 * c3) + c4))+1][c3]);
       for (c5 = c3; c5 <= min((N + -1), ((256 * c0) + 255)); c5++) {
        A[(M-2)-(((-1 * c3) + c4))][c5] = c[((-1 * c3) + c4)][c3]
                                          * A[(M-2)-(((-1 * c3) + c4))][c5]
                                          - s[((-1 * c3) + c4)][c3]
                                          * A[(M-2)-(((-1 * c3) + c4))+1][c5];
        A[(M-2)-(((-1 * c3) + c4))+1][c5] = s[((-1 * c3) + c4)][c3]
                                            * A[(M-2)-(((-1 * c3) + c4))][c5]
                                            + c[((-1 * c3) + c4)][c3]
                                            * A[(M-2)-(((-1 * c3) + c4))+1][c5];
  } } } }
    if (c0 <= (c2 + -1)) {
     for (c3 = (256 * c0);c3 <= min((M + -2),((256 * c0) + 255));c3++){
      for (c4 = max((256 * c1), c3);c4 <= min((M + -2),((256 * c1) + 255));c4++){
       for (c5 = (256 * c2); c5 <= min((N + -1), ((256 * c2) + 255)); c5++) {
        A[(M-2)-(((-1 * c3) + c4))][c5] = c[((-1 * c3) + c4)][c3]
                                          * A[(M-2)-(((-1 * c3) + c4))][c5]
                                          - s[((-1 * c3) + c4)][c3]
                                          * A[(M-2)-(((-1 * c3) + c4))+1][c5];
        A[(M-2)-(((-1 * c3) + c4))+1][c5] = s[((-1 * c3) + c4)][c3]
                                            * A[(M-2)-(((-1 * c3) + c4))][c5]
                                            + c[((-1 * c3) + c4)][c3]
                                            * A[(M-2)-(((-1 * c3) + c4))+1][c5];
       }  }  } } }  } } }
```

Fig. 16: Modified and automatically tiled Givens Rotation



(a) (b)

Fig. 17: Givens Rotation: performance improvements due to tiling

```
for (j = 0; j < N; j++) {
  total = 0;
  for (i = j+1; i < M; i++) {
    total += A[i][j] * A[i][j];
  }
  norm_x = (A[j][j] * A[j][j] + total);
  if (norm_x != 0) {
    if (A[j][j] < 0)
      norm_x = -norm_x;
    v[j] = norm_x + A[j][j];
    norm_v = (v[j] * v[j] + total);
    v[j] /= norm_v;
    for (i = j+1; i < M; i++) {
      v[i] = A[i][j] / norm_v;
    }
    for (jj = j; jj < N; jj++) {
      dot = 0.;
      for (kk = j; kk < M; kk++) {
        dot += v[kk] * A[kk][jj];
      }
      for (ii = j; ii < M; ii++) {
        A[ii][jj] -= 2 * v[ii] * dot;
      }
    }
  }
}
```

Fig. 18: Householder computation

total number of arithmetic operations to be performed. Indeed, on hardware where the computation power becomes increasingly cheaper relative to data access costs, standard complexity analysis alone is insufficient to capture the relative merits of alternative algorithms for a computation such as QR decomposition.

Analysis. Fig. 19 shows the reuse distance profile of the original code and the convex-partitioning for the Householder algorithm, for an input matrix of size 30 by 30.

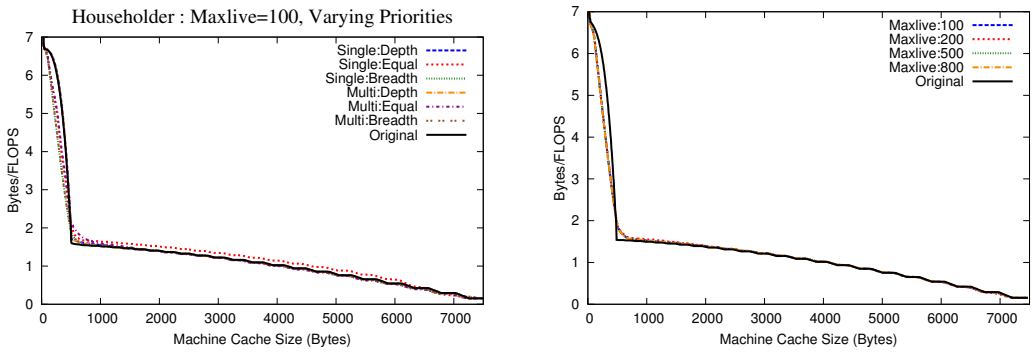


Fig. 19: Results with different heuristics for Householder

We observe a significant difference compared with Givens: the gap between the reuse distance profile of the original code and that found by our dynamic analysis is negligible. From this we conclude that the potential for data locality improvement of this algorithm is limited, and therefore we did not seek an optimized implementation for it.

Furthermore, comparing the bytes/flop required with the Givens graph in Fig. 14 shows that our tiled implementation of Givens achieves a significantly lower byte/flop ratio, especially for small

cache sizes. We conclude that the Givens rotation algorithm may be better suited for deployment on future hardware, because of its lower bandwidth demand than Householder, especially for small cache sizes.

4.3.4. Lattice-Boltzmann Method.

Original program. Fig. 20 shows the compute-intensive part within *470.lbm*, a SPEC2006 [Henning 2006; Pohl] benchmark. It implements the Lattice-Boltzmann technique to simulate fluid flow in 3 dimensions, in the presence of obstacles. The position and structure of the obstacles are known only at run-time, but do not change throughout the course of the computation.

The kernel shown in Fig. 20 iterates over points in a 3D cubic grid. At every point in this iteration space, the elements of the output array `dstGrid` are updated using a 19-point stencil (to compute `rho`) and three 10-point stencils (to compute `ux`, `uy` and `uz`). Automatically tiling of the code by current compilers is inhibited by the presence of i) the conditional at line 4 which checks for the position of obstacles, and ii) the output dependences due to updates to multiple locations of array `dstGrid` at every iteration point.

```
1.  for( k = 0 ; k < SIZE_Z ; k++)
2.    for( j = 0 ; j < SIZE_Y ; j++)
3.      for( i = 0 ; i < SIZE_X ; i++ ){
4.        if( is_obstacle(k,j,i) ){
5.          dstGrid[k][j][i] = srcGrid[k][j][i];
6.          dstGrid[k][j][i+1] = srcGrid[k][j][i+1];
7.          ...;
8.          continue;
9.        }
10.       rho = srcGrid[k][j][i] + srcGrid[k][j][i+1] + ...;
11.       ux = srcGrid[k][j][i+1] - srcGrid[k][j][i-1] + ...;
12.       uy = srcGrid[k][j+1][i] - srcGrid[k][j-1][i] + ...;
13.       uz = srcGrid[k+1][j][i] - srcGrid[k-1][j][i] + ...;
14.       ...;
15.       u2 = ux*ux + uy*uy + uz*uz;
16.       dstGrid[k][j][i] = a * srcGrid[k][j][i] + b * rho * ( 1 - u2);
17.       dstGrid[k][j][i+1] = a * srcGrid[k][j][i+1] + c * rho * ( 1 - u2);
18.       ...;
19.     }
```

Fig. 20: Representative computation in 470.lbm

Analysis. The convex-partition heuristics described in this paper are not constrained by either of the above restrictions, and are able to find valid operation reordering with enhanced data locality, as shown Figure 21. The "test" input size provided by the SPEC benchmark suite was used for the analysis. To reduce the size of the generated trace the problem size was reduced by a factor of 4 along each dimension.

For a cache size of 60KB, the reordering after convex obtained by the heuristics show improvement in the Bytes/FLOP ratio. For this benchmark all configurations of the heuristics yield essentially identical results. However, unlike the previous benchmarks, the absolute value of the bytes/flop is extremely low (Figure 21), indicating that the computation is already compute-bound and a tiled version of the code would not be able to achieve significant improvements in performance over the untiled code. On an Intel Xeon E5640 with a clock speed of 2.53GHz, the untiled version already achieves a performance of 4GFLOPS. But since the current trend in hardware architecture suggests that the peak performance will continue to grow at a faster rate than the increase in main-memory bandwidth, it is reasonable to expect that optimizations like tiling that improve data locality will be critical in the future even for such computations that are currently compute-bound.

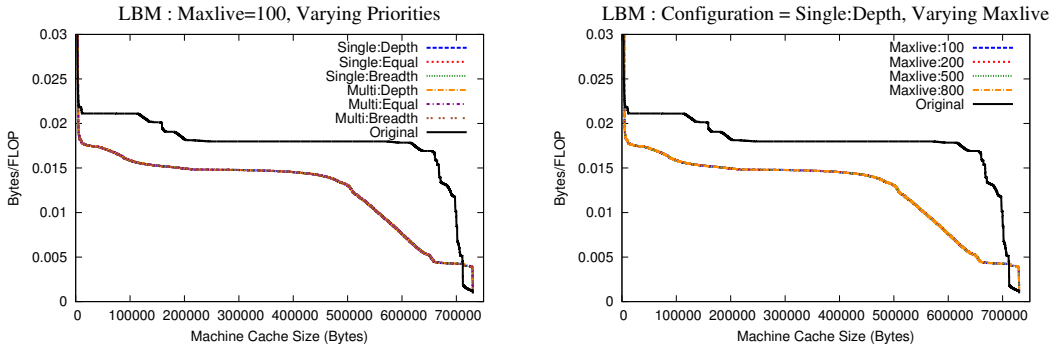


Fig. 21: Results with different heuristics for 470.lbm

4.3.5. 410.bwaves. This benchmark is a computational fluid dynamic application from SPEC2006 [Henning 2006]. We ran our analysis on the whole benchmark with "test" input size. For this benchmark too, the size of the problem was reduced by a factor of 4 along each dimension. For the sake of space saving we omit the benchmark code. The analysis results are shown in Fig. 22.

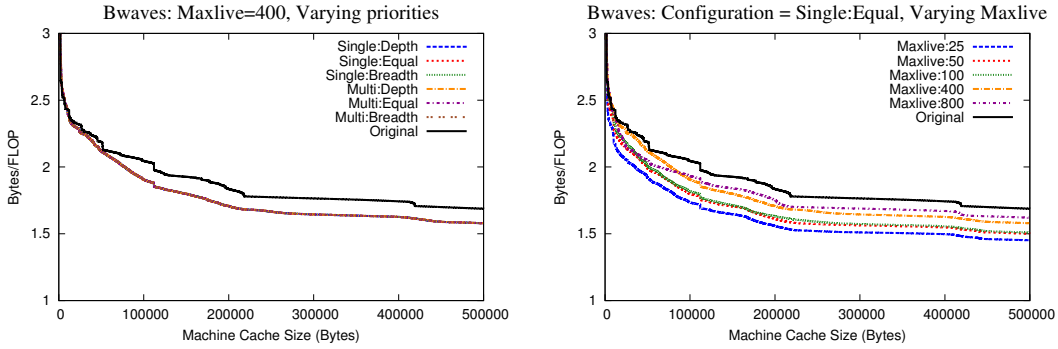


Fig. 22: Results with different heuristics for 410.bwaves

The analysis shows there is only a small potential data locality improvement that could be expected.

4.3.6. Large-Eddy Simulations with Linear-Eddy Model in 3D. 437.leslie3d is another computational fluid dynamic benchmark from SPEC2006 [Henning 2006]. We performed the analysis using the "test" dataset as given. As shown in Fig. 23, leslie3d achieves a lower bytes/FLOP ratio with the multi-level algorithm. The trend is not sensitive to varying Maxlive. Therefore, from the results, we conclude that this benchmark has high potential for locality improvement. We however leave for future work the task of deriving an optimized implementation for leslie3d.

4.3.7. Odd-Even Sort.

Original program. Our dynamic analysis does not impose any requirement on the data layout of the program: arrays, pointers, structs etc. are seamlessly handled as the trace extraction tool focuses exclusively on the address used in memory read/write operations. To illustrate this we show in Fig. 24 the original code for an odd-even sorting algorithm, using a linked-list implementation.

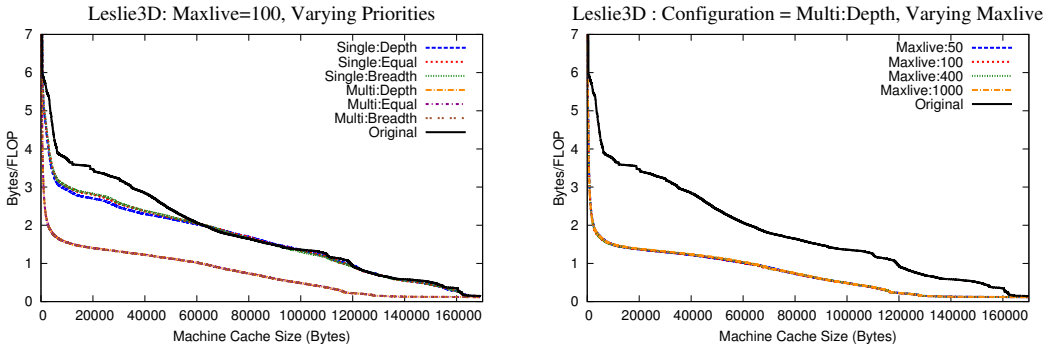


Fig. 23: Results with different heuristics for 437.leslie3d

`CompareSwap` compares the data between two consecutive elements in the list, and swaps them if necessary. There is a node in the CDAG for each swap operation.

```
for(i=0; i<N/2; ++i) {
  node *curr;
  for(curr=head->nxt; curr->nxt; curr=curr->nxt->nxt) {
    CompareSwap(curr, curr->nxt);
  }
  for(curr=head; curr; curr=curr->nxt->nxt) {
    CompareSwap(curr, curr->nxt);
  }
}
```

Fig. 24: Odd-Even sort on linked list

Analysis. Fig. 25 shows the reuse distance profile of the original code and its convex-partitioning for the odd-even sort, for a random input of size 256. As we can see from Fig. 25, the convex-partitioning heuristics shows significant potential for data locality improvement.

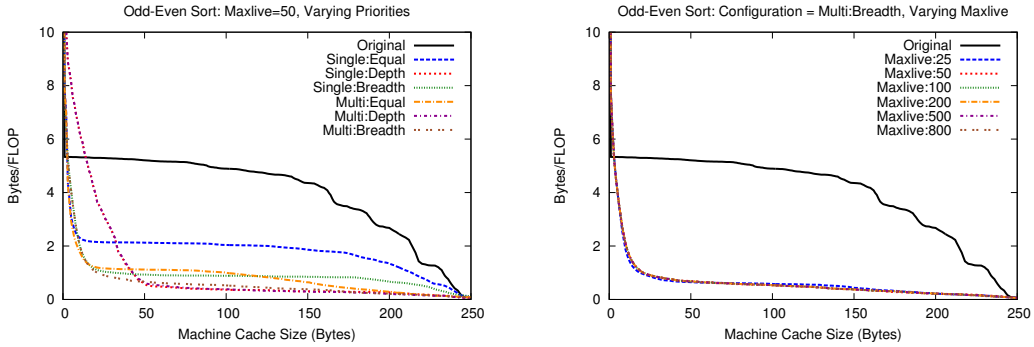
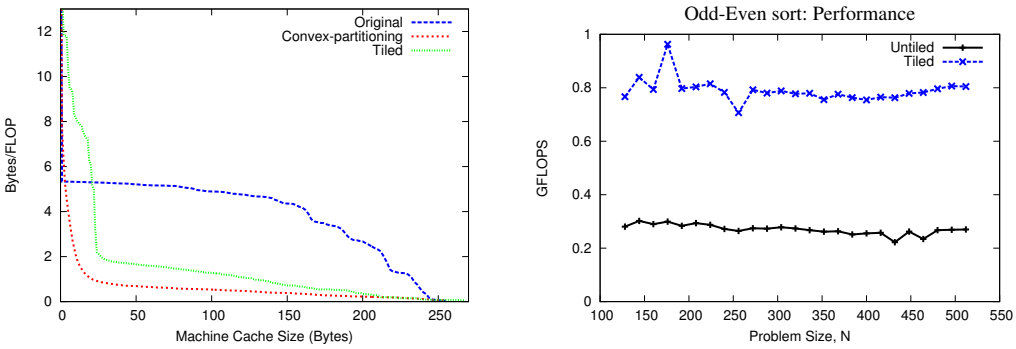


Fig. 25: Results with different heuristics for Odd-Even sort

Modified implementation. Based on careful analysis of the original code in Fig. 24, an equivalent register-tiled version with a tile size of 4 was manually developed, it is shown in Fig. 26.

```
register float Ra, Rb, Rc, Rd;
node *tail0, *tail1, *tail2, *tail3;
tail0 = tail;
tail1 = tail = tail->prev;
tail2 = tail = tail->prev;
tail3 = tail = tail->prev;

// Upper left part of the iteration space
node *curr = head;
for (I=0; I<N; I+=4) {
  ptr0 = curr;  Ra = ptr0->data;
  ptr1 = ptr0->nxt;  Rb = ptr1->data;
  ptr2 = ptr1->nxt;  Rc = ptr2->data;
  ptr3 = ptr2->nxt;  Rd = ptr3->data;
  curr = ptr3->nxt;
  // Full tiles
  for (T=I; T>0; T-=4) {
    CompareSwap(Ra, Rb); CompareSwap(Rc, Rd);
    ptr3->data = Rd; ptr3 = ptr0->prev; Rd = ptr3->data;
    CompareSwap(Rd, Ra); CompareSwap(Rb, Rc);
    ptr2->data = Rc; ptr2 = ptr3->prev; Rc = ptr2->data;
    CompareSwap(Rc, Rd); CompareSwap(Ra, Rb);
    ptr1->data = Rb; ptr1 = ptr2->prev; Rb = ptr1->data;
    CompareSwap(Rb, Rc); CompareSwap(Rd, Ra);
    ptr0->data = Ra; ptr0 = ptr1->prev; Ra = ptr0->data;
  }
  // Half tile corresponding to T==0
  CompareSwap(Ra, Rb); CompareSwap(Rc, Rd);
  ptr3->data = Rd;
  CompareSwap(Rb, Rc);
  ptr2->data = Rc;
  CompareSwap(Ra, Rb);
  ptr1->data = Rb;
  ptr0->data = Ra;
}
// Lower right part of the iteration space
for (I=4; I<=N; I+=4) {
  // Half tile corresponding to T==N
  ptr3 = tail0; Rd = tail0->data;
  ptr2 = tail1; Rc = tail1->data;
  CompareSwap(Rc, Rd);
  ptr1 = tail2; Rb = tail2->data;
  CompareSwap(Rb, Rc);
  ptr0 = tail3; Ra = tail3->data;
  // Full tiles
  for (T=N-4; T>=I; T-=4) {
    CompareSwap(Ra, Rb); CompareSwap(Rc, Rd);
    ptr3->data = Rd; ptr3 = ptr0->prev; Rd = ptr3->data;
    CompareSwap(Rd, Ra); CompareSwap(Rb, Rc);
    ptr2->data = Rc; ptr2 = ptr3->prev; Rc = ptr2->data;
    CompareSwap(Rc, Rd); CompareSwap(Ra, Rb);
    ptr1->data = Rb; ptr1 = ptr2->prev; Rb = ptr1->data;
    CompareSwap(Rb, Rc); CompareSwap(Rd, Ra);
    ptr0->data = Ra; ptr0 = ptr1->prev; Ra = ptr0->data;
  }
  ptr0->data = Ra; ptr1->data = Rb; ptr2->data = Rc; ptr3->data = Rd;
}
```

Fig. 26: Tiled odd-even sort



(a) (b)

Fig. 27: Odd-Even sort: Performance improvements due to tiling

Performance comparison. The comparison of performance of the untiled and tiled versions of the code is shown in Fig. 27.

Fig. 27a shows the improved data locality for the tiled code compared to the original code. The actual improvement in performance of the tiled code is shown in Fig. 27b for a random input. Experiments about sensitivity to datasets reported in later Sec. 4.4 confirm that our optimized variant consistently outperform the original code.

4.3.8. LU Decomposition (LAPACK). The last benchmark we analyze is a LU decomposition implementation for dense matrix, from the LAPACK package [Anderson et al. 1999]. It uses pivoting (therefore the computation is input-dependent) and LAPACK provides both a base implementation meant for small problem sizes, and a block decomposition for large problem sizes [LAPACK]. Both code versions can be found in [Anderson et al. 1999].

Fig. 28 shows the result of our dynamic analysis on the non-blocked implementation of LU decomposition, for a single random matrix of size 128 by 128. Additional experiments on dataset sensitivity are shown in later Sec. 4.4.

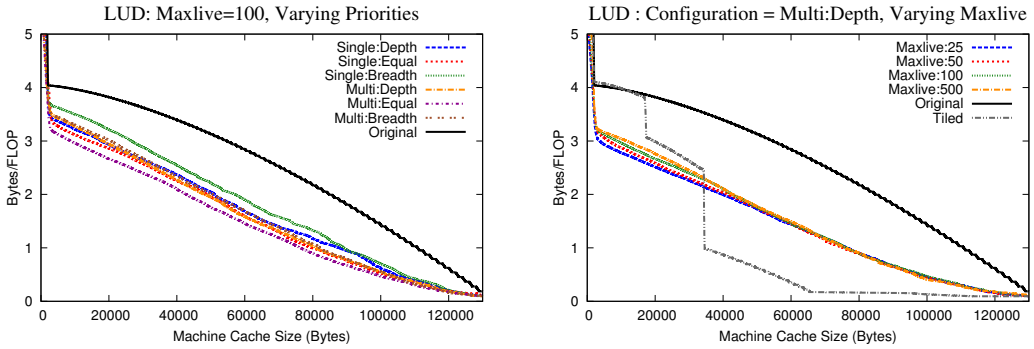


Fig. 28: Results with different heuristics for LUD

A potential for locality improvement is established from the result of the analysis. On Fig. 28b we additionally plotted the profile of tiled (i.e., blocked) implementation, in addition to the original (i.e., non-blocked) one. The blocked version shows a better bytes/Flop than the convex partitioning for cache sizes larger than 35kB, this is likely due to inter-block reuse achieved in the highly optimized

LAPACK implementation; together with a sub-optimal schedule found by our heuristic. Further, Fig. 29b shows actual performance, in GFLOPS, for non-blocked and blocked versions of the code.

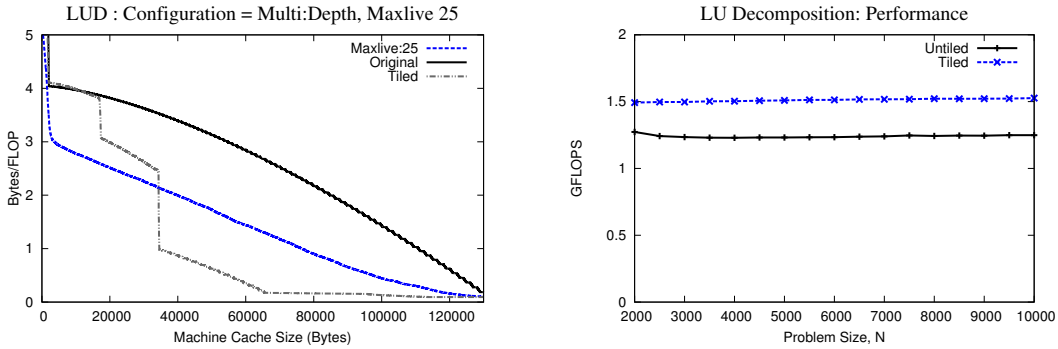


Fig. 29: LU Decomposition

4.4. Dataset Sensitivity Experiments

We conclude our experimental analysis with a study of the sensitivity of our analysis to different datasets. In the set of benchmarks presented in the previous section, the majority of them have a CDAG which depends only on the input dataset size, and not on the input values. Therefore for these codes our dynamic analysis results hold for any dataset of identical size.

Odd-even sort and LUD are two benchmarks which are input-dependent. To determine the sensitivity of the convex-partitioning heuristics on the input, we ran the heuristics on different datasets, as shown in Fig. 30 and Fig. 31.

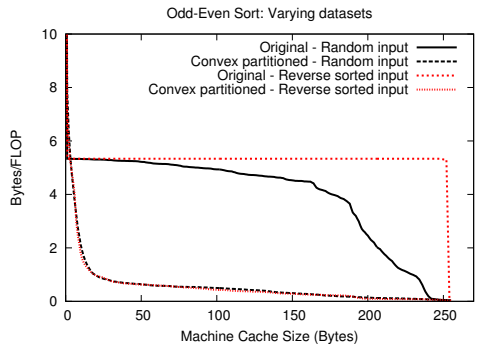


Fig. 30: Sensitivity analysis for odd-even sort

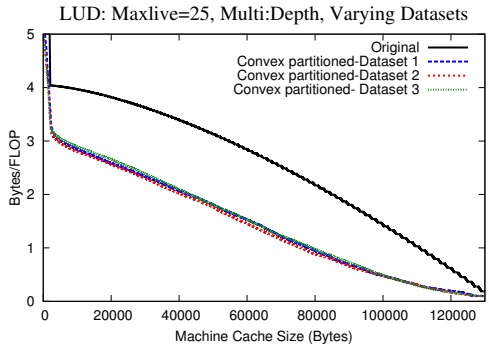


Fig. 31: Sensitivity analysis for LUD

Fig. 30 shows the result for two such datasets - one with random input elements and the other with the reverse sorted input list, a worst-case dataset. We used multi-level heuristics with breadth-first priority, which corresponds to the parameters of the best result, which can be found in [Fauzia et al. 2013]. As we can see from Fig. 30, the potential for improvement exhibited by the heuristics remains consistent when varying inputs: the “Convex partitioned” reuse distance profile does not vary with the input value. We note that in the general case, some variations are expected for different datasets,

and similarly to complexity analysis of such algorithms, one needs to perform both worst-case analysis (i.e., reverse-sorted) and analysis on random/representative datasets for best results.

Fig. 31 exhibits a similar behavior where the three tested datasets have a similar analysis profile. The first dataset has is a random matrix, the second was created so that the pivot changes for about half the rows of the matrix, and for the third one the pivot changes for all rows of the matrix.

5. RELATED WORK

Both algorithmic approaches (e.g., [Demmel et al. 2012; Ballard et al. 2011a; 2011b]) and compiler transformations (e.g., [Irigoin and Triolet 1988; Wolf and Lam 1991; Kennedy and McKinley 1993; Bondhugula et al. 2008]) have been employed to improve data locality. The applicability of these techniques to arbitrary computations is limited. For example, compiler optimizations typically require programs in which precise static characterization of the run-time behavior is possible; this is challenging in the presence of inter-procedural control flow, diverse data structures, aliasing, etc. Reuse distance analysis [Mattson et al. 1970; Ding and Zhong 2003], which considers the actual observed run-time behavior, is more generally applicable and has been used for cache miss rate prediction [Zhong et al. 2003; Marin and Mellor-Crummey 2004; Jiang et al. 2010], program phase detection [Shen et al. 2004], data layout optimizations [Zhong et al. 2004], virtual memory management [Cascaval et al. 2005], and I/O performance optimizations [Jiang and Zhang 2005]. Even though reuse distance analysis provides insights into the data locality of software behavior, it has been limited to analyzing locality characteristics for a specific execution order of the operations, typically that generated by a sequential program. In contrast to all previous work on reuse distance analysis, to the best of our knowledge, our upper-bounding approach is the first to attempt a schedule-independent characterization of the inherent data locality characteristics of a CDAG.

The idea of considering valid re-orderings of a given execution trace has been applied successfully to characterize the potential parallelism of applications. Kumar's approach [Kumar 1988] computes a possible valid schedule using a timestamping analysis of an instrumented statement-level execution of the sequential program. Shadow variables are used to store the last modification times for each variable. Each run-time instance of a statement is associated with a timestamp that is one greater than the last-modify times of all its operands. A histogram of the number of operations at each time value provides a fine-grained parallelism profile of the computation, and the maximal timestamp represents the critical path length for the entire computation. Other prior efforts with a similar overall approach include [Austin and Sohi 1992; Nicolau and Fisher 1984; Kumar 1988; Wall 1991; Lam and Wilson 1992; Theobald et al. 1992; Rauchwerger et al. 1993; Postiff et al. 1999; Stefanović and Martonosi 2000; Mak and Mycroft 2009; Garcia et al. 2011].

In contrast to the above fine-grained approach, an alternate technique developed by Larus [Larus 1993] performed analysis of loop-level parallelism at different levels of a nested loop. Loop-level parallelism is measured by forcing a sequential order of execution of statements within each iteration of a loop being characterized, so that the only available concurrency is across different iterations of that loop. A related technique is applied in the context of speculative parallelization of loops, where dynamic dependences across loop iterations are tracked [Rauchwerger and Padua 1995]. A few recent approaches of similar nature include [Bridges et al. 2007; Tian et al. 2008; Zhong et al. 2008; Wu et al. 2008; Oancea and Mycroft 2008; Tournavitis et al. 2009]. In order to estimate parallel speedup of DAGs, Sarkar and Hennessy [Sarkar and Hennessy 1986] developed convex partitioning of DAGs. In previous work, we [Holewinski et al. 2012] used dynamic analysis of CDAGs to assess the vectorization potential of codes that are not effectively vectorized by current vectorizing compilers. However, we are not aware of any prior work on dynamic analysis of CDAGs with the goal of characterizing and/or enhancing data locality properties of computations.

6. DISCUSSION

In this section, we discuss the potential and some of the current limitations of the dynamic analysis approach for data locality characterization/enhancement that we have developed in this article.

Dependence on Input Values. As with any work that uses dynamic analysis of the actual execution trace of a program, any conclusions drawn are only strictly true for that particular execution. For programs where the execution trace is dependent on input data, the CDAG will change for different runs. For many programs, including all the benchmarks evaluated in this paper, the CDAG is independent of the numerical values of the input data, but clearly varies with the size of the problem, e.g., size of the matrices used in the code. Due to space limitations, we only present RDA results for a single problem size for each benchmark. However, we have experimented with different problem sizes and the qualitative conclusions remain stable across problem size. Further, as demonstrated by the case studies of the Floyd-Warshall and Givens rotation codes, the modified codes based on insights from the dynamic analysis were demonstrated to exhibit consistent performance improvement for different problem sizes.

Overhead of Analysis. The initial prototype implementation of the partitioning algorithm has not yet been optimized and currently has a fairly high overhead (about 4 orders of magnitude) over the execution time of the analyzed program. As discussed earlier, the computational complexity of the partitioning algorithm is $O(|T|)$ for the single-level version, and $O(|T|\log(|M|))$ for the multi-level version and can therefore be made sufficiently efficient to be able to analyze large-scale applications in their entirety. A more significant challenge is the space requirement, since the size of a CDAG is often much larger than the combined space for the instructions and data structures of the analyzed computation. The development of an "out-of-core" analyzer is the focus of ongoing follow-up work. Another solution is to compress the CDAG using a technique similar to trace compression [Ketterlin and Clauss 2008] leading to a space complexity of $O(|M|+|P|)$ in the most favorable scenario (in which all dependences turn out to be affine). More generally trace sampling techniques can be applied to tackle scalability issues of this approach.

Tightness of Estimation. The primary goal of our CDAG partitioning algorithm is to find a more favorable valid reordering of the schedule of its operations so as to lower the needed volume of data movement between main memory and cache. From the perspective of data movement, the lowest possible amount, corresponding to the best possible execution order for a given CDAG and a given cache size, can be considered the *inherent data access complexity* of that computation. But, irrespective of how much lower the reordered schedule's data movement volume is compared to the original schedule's data movement volume, how do we determine how close we are to the data volume for the best possible valid order of execution? A solution to this problem is to work in the opposite direction and develop lower bound techniques for the data access complexity of CDAGs. In complementary concurrent work in progress, we are developing an approach to establishing lower bounds on the data movement costs for arbitrary CDAGs. One way of assessing the tightness of the upper bounds (this work) and lower bounds (complementary work in progress) is to see how close these two bounds for a given CDAG are.

Use of Analysis. We envision several uses of a tool based on the dynamic analysis approach developed in this paper. (1) *Application Developers*: by running the dynamic analysis on different phases of an application, along with standard performance profiling, it is possible to identify which of the computationally dominant phases of the application may have the best potential for performance improvement through code changes to enhance data reuse. Dynamic analysis for data locality can also be used to compare and choose between alternate equivalent algorithms with the same functionality – even if they have similar performance on current machines. If the reuse distance profiles of two algorithms after reordering based on dynamic analysis are very different, the algorithm with lower bandwidth demands would likely be better for the future. (2) *Compiler Developers*: compilers implement many transformations like fusion and tiling that enhance data reuse. The dynamic analysis tool can be used to gauge the separation between the reuse distance profile after compiler transformation with that from convex partitioning on the CDAG. A significant separation indicates potential for improvement of the compiler transformation system. (3) *Architecture Design*: running the dynamic analysis tool on a collection of representative applications can guide vendors of archi-

tectures in designing hardware that provides adequate bandwidth and/or sufficient capacity at the different levels of the memory hierarchy.

7. CONCLUSION

With future systems, the cost of data movement through the memory hierarchy is expected to become even more dominant relative to the cost of performing arithmetic operations [Bergman et al. 2008; Fuller and Millett 2011; Shalf et al. 2011], both in terms of throughput and energy. Therefore optimizing data locality will become ever more critical in the coming years. Given the crucial importance of optimizing data access costs in systems with hierarchical memory, it is of great interest to develop tools and techniques for characterization and enhancement of the data locality properties of an algorithm. Reuse distance analysis is a widely used approach to model data locality [Mattson et al. 1970; Ding and Zhong 2003] in computations. Although reuse distance analysis provides a useful characterization of data locality for a given execution trace, it fails to provide any information on the potential for improvement in data reuse that may be feasible through valid reordering of the operations in the execution trace.

In this paper, we have developed a dynamic analysis approach to provide insights beyond that possible from standard reuse distance analysis. Given an execution trace from a sequential program, we seek to (i) characterize the data locality properties of an algorithm and (ii) determine if there exists potential for enhancement of data locality through execution reordering. Instead of simply performing reuse distance analysis on the execution trace of a given sequential program, we first explicitly construct a dynamic computational directed acyclic graph (CDAG) to capture the statement instances and their inter-dependences, perform convex partitioning of the CDAG to generate a modified dependence-preserving execution order with better expected data reuse, and then perform reuse distance analysis for an address trace corresponding to the modified execution order. We have demonstrated the utility of the approach in characterizing/enhancing data locality for a number of benchmarks.

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